SAGE 2X00 Operation & Maintenance Manual

S2X00-AAA-00001 V1.0

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For Reference Only

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1 Introduction

This user manual describes the operation and maintenance of the SAGE 2400 Remote Terminal Unit (RTU).

The SAGE 2400 Remote Terminal Unit is designed to satisfy a wide range of Supervisory Control and Data Acquisition (SCADA) application requirements in harsh environmental conditions.

The SAGE 2400 Graphical User Interface guides the user through setup and operation while expanding the rich functionality you have come to expect from SAGE RTUs.

The Theory of Operation chapter should be used in conjunction with the SAGE 2000 Operation & Maintenance manual (C3400-AAA-00002), which contains complete schematics and printed circuit assembly drawings. The drawings also include bills of material for those users wishing to perform component level repair of failed assemblies.

1.1 Features

The SAGE 2400 uses the latest electronic technology for reliability, speed and maintainability. It is intended for use in a variety of SCADA applications requiring maximum configuration flexibility. The design includes several state-of-the-art functional capabilities. For example, the AC Input (ACI) option provides an advanced transducer-less AC analog input capability.

The SAGE 2400 has the following new features:

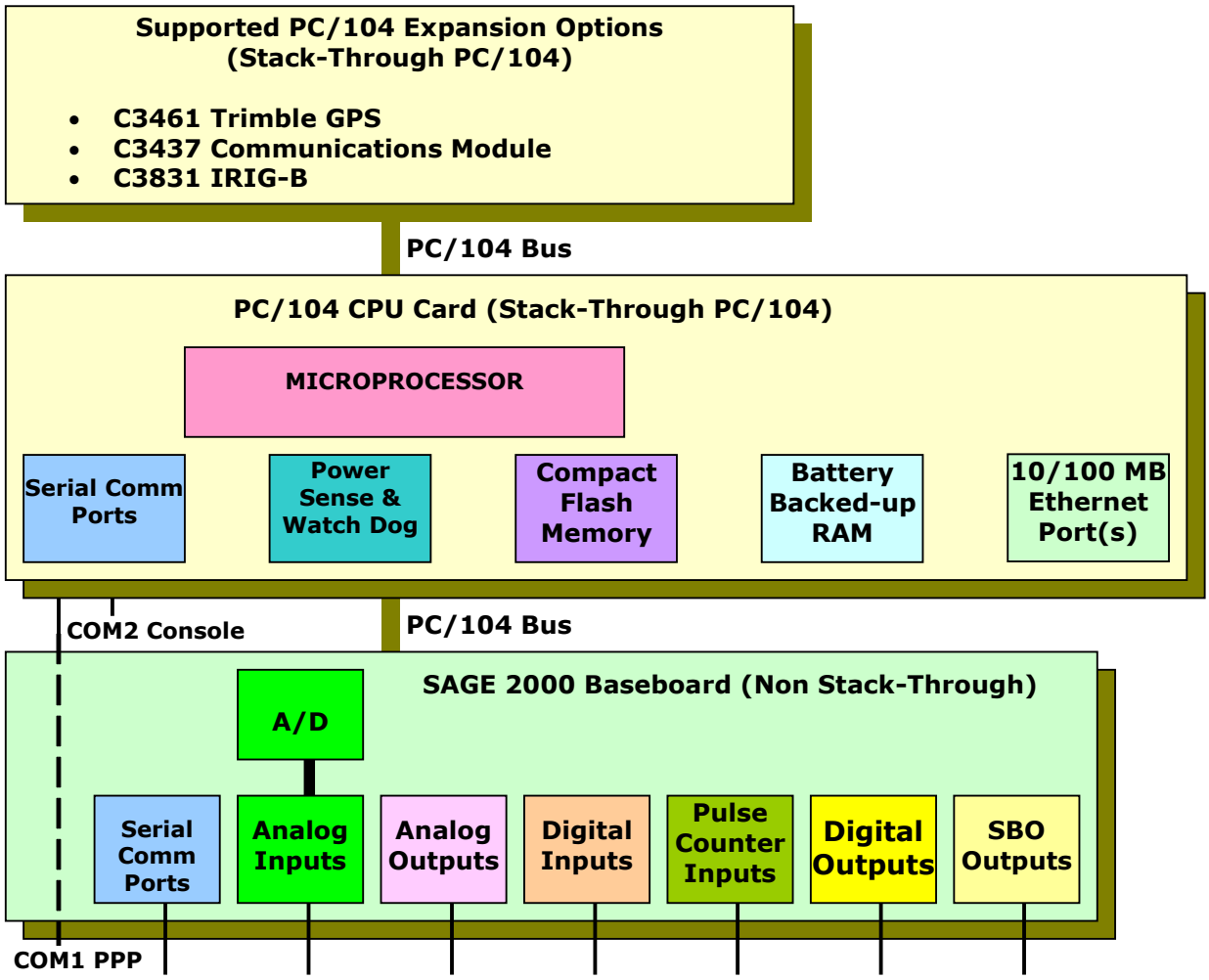
- Easy-to-use Graphical User Interface (GUI) via Microsoft Internet Explorer
- Embedded web server
- Built-in Ethernet with TCP/IP
- File Transfer Protocol (FTP)
- May be configured either locally or remotely
- Point naming (no more counting point numbers to find your point of interest)
- Point mapping with simple click and drop
- Data concentration – adds data from multiple IEDs to one database for fast polling
- Protocol conversion – convert multiple protocols to a standard protocol
- Built on a widely adopted Real-Time Operating system (RTOS)
- Employs standard PC/104 bus interface for CPU and communication upgrades
- Relay Ladder Logic capability that supports all five IEC 61131-3 languages
- Provides Upgrade path for SAGE 2100 and Micro/1C products

1.2 Architecture

Figure 1-1 shows a simplified block diagram of the SAGE 2400 Baseboard which illustrates its general architecture and major components. The basic SAGE 2400 consists of a Baseboard, a microprocessor daughter board, and additional XTs as required to satisfy specific system needs. All address and control selection signals needed for the XTs are generated on the Baseboard. Terminal block connections are provided for all external I/O lines.

Additionally, the open architecture of the PC/104 interface provides for expanded functions. You may add a PC/104 GPS receiver and/or C3437/C3438 Communication cards that allow up to eight additional Communication ports.

Figure 1-1 SAGE 2400 Simplified Block Diagram



1.3 Graphical User Interface (GUI)

The SAGE 2400 is easily configured using the standard web browser, Internet Explorer version 6.0 or later. The physical connection may be made in one of four ways:

- Ethernet connection using an Ethernet crossover cable directly to the CPU card
- Ethernet connection to a network , locally or remotely
- PPP connection using a null-modem cable to the UIF port
- Console – this method commonly used to read and/or change IP address

See Appendix A for details on connections.

The GUI is designed around the classical client/server model. A web browser is all you need for your client (PC) and you can browse any RTU product or any version of that product that supports our web interface. All configuration data is stored on the RTU in the form of Extensible Markup Language (XML). XML data is served up to the browser within HTML pages or transformed into HTML via Extensible Stylesheet Language (XSL). In either case data is presented to the user in an intuitive format using common design elements like forms, Radio Buttons, Spin Boxes, Alert Boxes, etc. for much of the data entry.

The GUI supports File Transfer Protocol (FTP), or SFTP on the Secure Firmware, to transfer files to/from the RTU and the client. The file types include RTU applications, Web pages, Configuration files, and the

Operating system. In short, every file within one RTU can be transferred to another RTU or parts of the RTU file system can be upgraded as needed. This provides a powerful means of performing firmware upgrades or configuration changes.

General Operational Considerations

Note: See the config@WEB Software Users Guide for initial user name and password.

Note: The initial TCP/IP address is 172.18.150.50.

Note: For the latest firmware, please see our website at https://infrastructurecommunity.schneider-electric.com/community/products/sage

1.4 Point Mapping

The RTUs of today must interface to a wide Varity of I/O and industry standard IEDs. This creates within the RTU a large database of points that have been acquired by the RTU that must be transferred to one or more master stations.

The SAGE 2400 GUI supports an intuitive drag and drop point mapping scheme. Each point within the RTU is named and scaled with user definable names and values. Scaling is used for local data display as well as protocol count scaling for conversion of data from one protocol to another.

1.5 Communications

The SAGE 2400 supports a large suite of communication protocols over many different types of communications media. Ethernet and RS232 come as standard hardware. However, installation of media converters allow for just about any physical communications media to be supported.

The UIF is a dedicated RS-232 port that supports a connection to the operating system using a terminal emulation program. It is used to configure the customer RTU IP and to change to safe mode operation. Diagnostic functions may also be performed using this port.

A second RS-232 port is available that supports the Point to Point Protocol (PPP). This port can perform all GUI functions, but at a 38.4kb.

Both ports can be used concurrently with the other serial and Ethernet ports.

All SAGE RTU products support multiple RTU and IED protocols. This allows for data to be mapped from IEDs to multiple masters via different RTU protocols. Example: If you were replacing your current master station software that talks Series V protocol with a system that supports DNP your RTU could talk to both the old master and the new master at the same time. This provides an excellent means of replacing legacy RTU/MTU equipment without interruption to data acquisition.

An emerging need for RTU products is SCADA protocols to communicate over Ethernet all the way down to the RTU. The SAGE 2400 supports DNP3 and Modbus over Ethernet.

1.6 I/O And Communication Expansion

The SAGE 2400 is designed to be cost effective in a wide range of input/output configurations. The SAGE 2400 has a versatile Baseboard with built in points as follows:

- 8 analog inputs
- 16 digital inputs
- 4 Select Before Operate (SBO) control points or 8 digital outputs
- 2 high-speed Pulse Counter Inputs (PCIs)

- 4 configurable communications ports

The number of points can be easily expanded by the use of External Termination panels (XTs), including Sequence of Events (SOE) XTs accurate to one-millisecond time stamps. The combination of baseboard and XTs yields a total point count as follows:

- 232 analog inputs
- 240 digital inputs
- 128 SBO outputs
- 384 one millisecond Sequence of Events (SOE) points
- 12 analog outputs
- 66 PCIs
- 264 digital outputs
- 12 configurable communications ports

The SAGE 2400 can also be configured for AC Analog Inputs (ACI) by using an optional C3244 ACI card. ACI allows you to replace most conventional analog transducers and monitor power quality (sags and swells) and other AC events.

1.7 Relay Ladder Logic (RLL)

The SAGE 2400 supports a RLL Runtime Target that accepts applications that can be developed using any one of the five IEC 61131-3 languages plus flow Charting. Programs are developed on an application workbench that runs only on the client. Fully developed/debugged programs can be downloaded into the SAGE 2400 and activated for execution.

RLL applications have access to all the data within the RTU and make use of the powerful mapping capabilities of the GUI. Output data from RLL applications can be viewed in real time data displays.

1.8 Packaging

The SAGE 2400 Baseboard is mounted on a flat panel for installation in a NEMA style cabinet for small point count configurations. It also may be mounted on an EIA universal 19-inch rack mountable panel.

The XTs are available in an 8 x 5-inch panel mount version and a 19-inch rack mount version.

2 Specifications

2.1 User Computer Requirement

OPERATING SYSTEM	Windows XP or higher with Internet Explorer 6 or higher. If using XML to Excel macro, Microsoft Office 2003 or above.

2.2 Environmental

OPERATING TEMPERATURE	-40° to +85° C
RELATIVE HUMIDITY	5% to 95%, non-condensing
TRANSIENT PROTECTION	All user field connections designed to pass: IEEE 472-1974, ANSI C37.90-1979 (R1982) ANSI C37.90.1-1989

2.3 Analog Inputs

INPUT TYPE	Differential
INPUT RANGES	±5VDC, 0-5VDC, 1-5VDC, ±1mA, 0-1mA, 4-20mA, 10-50mA
RESOLUTION	13 bits (12 bits plus sign) – PCBs REV up to K 12 bits (11 bits plus sign) – PCBs REV M and up
COMPREHENSIVE ACCURACY	±0.1% FS between –40° and +85°C
DC POWER MEASUREMENT	2%
REFERENCE VOLTAGES	±4.500V
CONVERSION RATE	All analogs once per second
COMMON MODE RANGE	±10V
COMMON MODE REJECTION	80 dB @ 50/60Hz
NORMAL MODE REJECTION	60 dB @ 50/60Hz
INPUT RESISTANCE	10M ohm or greater
BASEBOARD POINTS	8
MAX INPUTS	232
CONFIGURATION	2 terminals per point (+ and -) with a shared shield ground.
XT DIMENSIONS	16pt 5x8 inch & 16pt 5.25x19 inch

2.4 AC Inputs

Warning: The applications Energy Calculation, Timing, and the ACI function all use the same BB ram memory space; therefore only one of these applications may be run at any given time.

Please refer to the C3244 AC Analog Input Option Manual (C3244-AAA-00011) for ACI specifications.

2.5 Analog Outputs

OUTPUT RANGE	0-1mA, 4-20mA, 10-50mA, ±5V, ±10V
ISOLATION	Optical, 1500 VDC, per board
RESOLUTION	12 bits
COMPREHENSIVE ACCURACY	±0.1% (from 0 to 50°C)
POWER LOSS PROTECTION	Outputs powered by external supply are protected from RTU power loss
CONFIGURATION	3 terminals per point
MAX OUTPUTS	12
XT DIMENSIONS	4pt 5x8 inch

2.6 Digital Inputs

2.6.1 Status Inputs

ISOLATION	Optically isolated, 1500VDC
LOOP VOLTAGES	12, 24, 48, and 129VDC
DEBOUNCE	20 msec nominal
CONFIGURATION	2 terminals per point (+ and -)
BASEBOARD POINTS	16
MAX INPUTS	240
POWER	Baseboard and XT excitation
INDICATORS	One LED per point.
XT DIMENSIONS	16pt 5x8 inch, 32pt 5x8 inch & 32pt 7x19 inch

2.6.2 Accumulator Inputs

ACCUM. FORMATS	FA, FC (1 or 2 counts/cycle)
ACCUM. INPUT RATE	20 pps max.
MAX INPUTS	240

2.6.3 SOE Inputs

ACCURACY	5ms, leading edge tagged
DEBOUNCE	20ms fixed
STORAGE CAPACITY	256 events, optional 1024

2.6.3.1 1 Millisecond SOE Inputs

ACCURACY	1ms, leading edge tagged
DEBOUNCE	20ms nominal (configurable)
STORAGE CAPACITY	256 events on XT, optional 1024
INPUT POWER	5W max, 3W typical.
XT DIMENSIONS	128 point 5x8 inch (requires DI XTs)
Maximum number of XTs	3 per baseboard

2.7 Pulse Counter Inputs

ISOLATION	Optically isolated, 1500VDC
LOOP VOLTAGES	12, 24, 48, 129VDC
ACCUMULATOR FORMATS	FA (1 count/cycle)
ACCUMULATOR INPUT RATE	10kHz max
INPUT FILTER	Hardware selectable 30Hz, 1kHz or 10kHz
CONFIGURATION	2 terminals per point (+ and -)
INPUTS	66 max, 2 on Baseboard and 64 on XTs
XT DIMENSIONS	8pt 5x8 inch

2.8 SBO Control Outputs

DURATION	Software programmable in 5 millisecond increments
CONTACT FORM & RATINGS	
BASEBOARD:	K20 type 1FC 20A @ 240VAC or 10A @ 28VDC
XT:	KUP type 1FC/2FA 10A @ 240VAC or 10A @28VDC. KUEP momentary type 1FC 3A @ 150VDC, 2FA 5A @ 150VDC, 1FX 10A @ 150 VDC. KUL latching type 1FC/2FA 10A @ 240VAC or 10A @28VDC.
RELAY INSTALLATION	Socketed
BASEBOARD POINTS	4 (from 8 DO points)
MAX OUTPUTS	128 (each output point is 2 relays)
CONTROL INHIBIT	Local/Remote switch on Baseboard
XT DIMENSIONS	4pt 6.4x8 inch & 8pt 8.75x19 inch

2.9 Digital Outputs

DURATION	Software programmable in 5 millisecond increments
CONTACT FORM & RATINGS	
BASEBOARD:	K20 type 1FC 20A @ 240VAC or 10A @ 28VDC
XT:	KUP type 1FC/2FA 10A @ 240VAC or 10A @28VDC. KUEP momentary type 1FC 3A @ 150VDC, 2FA 5A @ 150VDC, 1FX 10A @ 150 VDC, 1FC 10A @ 24VDC, 1FC 10A @ 12VDC
RELAY INSTALLATION	Socketed
BASEBOARD POINTS	8 (also configurable as 4 SBOs)
MAX OUTPUTS	264
INDICATORS	One LED per point
POWER	Baseboard points have coil excitation, XTs require wiring to DC supply
XT DIMENSIONS	16pt 5x8 inch & 32pt 7x19 inch

2.9.1 Alarm Outputs

CONTACT FORM & RATINGS	2FC 0.6A @ 125VAC or 0.6A @ 110VDC or 2.0A @ 30VDC (special application firmware required for customer implementation)

2.10 CPU/Memory

Please refer to the CPU Manual for CPU/Memory Specifications

2.11 Communications

NUMBER OF RS-232C PORTS	1 Console, 1 PPP User Interface, 4 Communications ports on baseboard, up to 8 additional ports with optional C3437 PC/104 cards and C3438 Comm Expansion card
SPEEDS	300-9600 bps
PROTOCOLS	Synchronous and asynchronous
ETHERNET	One built-in 10/100BASE-T (RJ45) auto-negotiate (will adjust to the speed and half/full duplex of the connecting device)

2.12 C3463 PCA Ethernet 10/100 5-Port Switching Hub (Optional)

ETHERNET	Five built-in 10/100BASE-T (RJ45) auto-negotiate (will adjust to the speed and half/full duplex of the connecting device)

2.13 Power Requirements

INPUT VOLTAGE	10 to 33VDC required by the Baseboard
OPTIONAL POWER SOURCES	120/240VAC with added supply/battery charger; 12VDC, 48VDC, 129VDC with added DC/DC supply
INPUT POWER	10.5W typ. for 10V to 33V for baseboard (excluding relays and analog current loops)
INPUT/OUTPUT ISOLATION	500 VDC
LOOP EXCITATION	Provided for Baseboard DIs, PCIs
BATTERY CHARGER	Optional external unit

2.14 Visual Indicators

BASEBOARD LEDs	Input Power LED Reset LED Local/Remote LED 5 LEDs per COMM port (DCD, RX, RTS, TX, CTS) Status Inputs LEDs (1 per input) PCI LEDs (2 each) Relays (1 per coil)
PC/104 CPU LEDs	Please refer to CPU Manual

3 Maintenance

This chapter describes calibration and maintenance procedures for the SAGE 2400. Those users who desire a more thorough technical understanding of the SAGE 2400 should refer to the Theory of Operation chapter which contains detailed descriptions of each module, and to the SAGE 2000 manual (C3400-AAA-00002), which contains complete schematics, bills of materials, and printed circuit board assembly drawings.

The following equipment is recommended for performing routine maintenance and repair on SAGE 2400 RTUs:

- Precision 4-1/2 digit DMM, (±0.01% accuracy)
- Thermometer, preferably digital

The SAGE 2400 requires very little routine adjustments, with the exception of analog input calibration. All adjustments, including calibration, are preset at the factory, and should not require calibration at startup.

3.1 Analog Input Calibration

The analog input section of the SAGE 2400 has a simple calibration technique that is intended for use while the RTU is operating on-site. The RTU has two dedicated internal references that provide 5V and 4.5V, which are used to calibrate the A/D. Since the RTU is generating these references, only a precision voltmeter and a small screwdriver are required to perform the calibration. See Figure 3-8 to locate adjustments and test points.

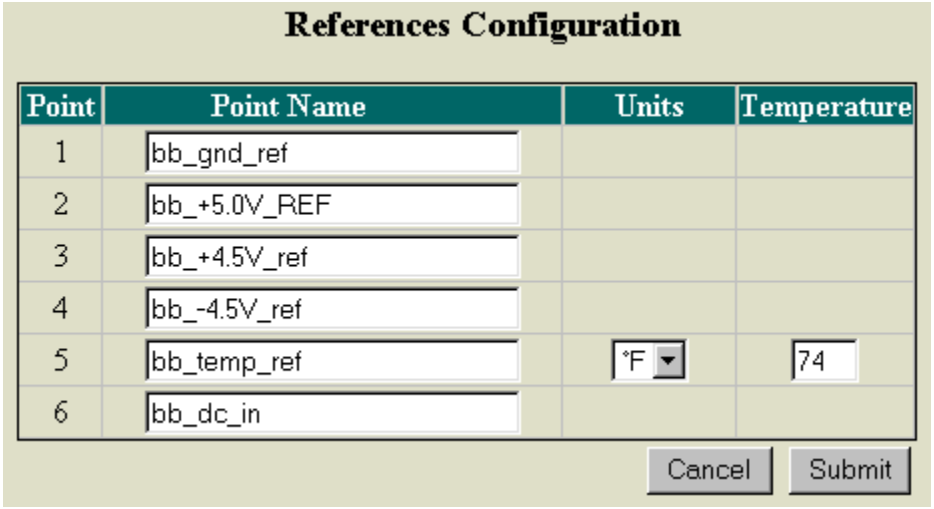
1. Connect the voltmeter between TP14 (analog ground) and TP13 (5V reference)
2. Adjust potentiometer R20 until the meter indicates 5.000 Volts ±0.001V.
3. Connect the voltmeter between TP14 (analog ground) and TP15 (4.5V reference).
4. Adjust potentiometer R19 until the meter indicates 4.500 Volts ±0.001V.

This ensures the internal ±100% and ±90% reference points are accurate.

3.2 Temperature Calibration

The References Configuration screen allows you to set the temperature units (°F or °C) and correct the temperature reading. This step should not be done remotely because you must enter the current correct temperature at the RTU. See Figure 3-1. Click Submit when you are satisfied with the configuration, or Cancel to back out of the function without saving.

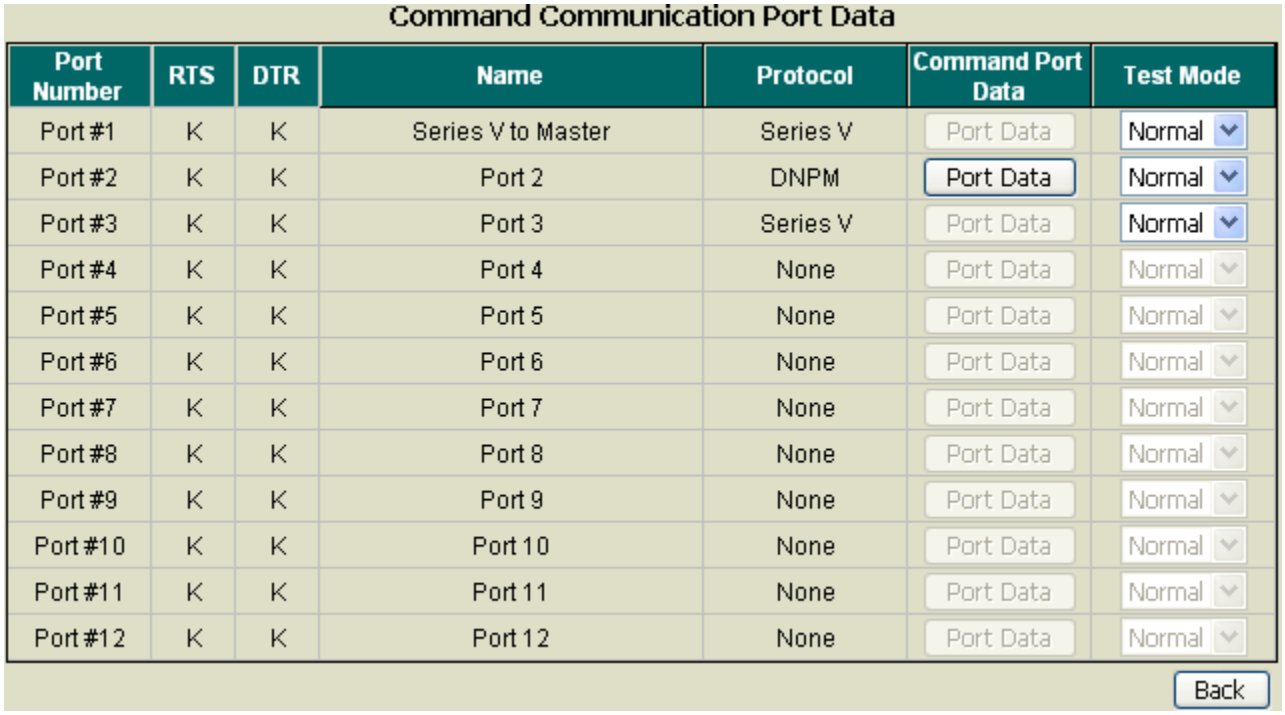
Figure 3-1 References Configuration



3.3 Comm Port Diagnostics

The RTU includes a built-in test routine that allows limited testing of the communication ports. Click the Command tab, then click Serial Comm. You will see a screen similar to Figure 3-2.

Figure 3-2 Command Communications Port Data



Under the Test Mode heading, select the type of test you wish from the pull-down menu for the port of interest. The choices and the meaning of each type of test is listed below. See Figure 3-4 for the expected results for each test.

Normal
In the normal mode, the selected comm channel functions normally. Each channel will be in this mode when the display is called up. Each channel is automatically restored to this mode when you exit from the display or the RTU is reset.

Mark
In the mark mode, the selected comm channel outputs a continuous stream of ones. Marks for the RS-232 channel are low (negative) voltage pulses, and low frequency (1,200Hz) for any attached 202 modem.

Space
In the space mode, the selected comm channel outputs a continuous stream of zeros. Spaces for the RS-232 channel are high (positive) voltage pulses, and high frequency (2,200Hz) for any attached 202 modem.

Alt
In the Alt mode, the selected comm channel outputs a continuous stream of alternating ones and zeros at the baud rate originally selected for the channel.

You may use a scope to see the outputs on the ports under test as shown in Figure 3-4. Notice that the test mode will terminate and return to Normal mode if you leave this screen with the pull-down menus in anything other than Normal, as shown in Figure 3-3.

Figure 3-3 Clicking the Back Button While in Test

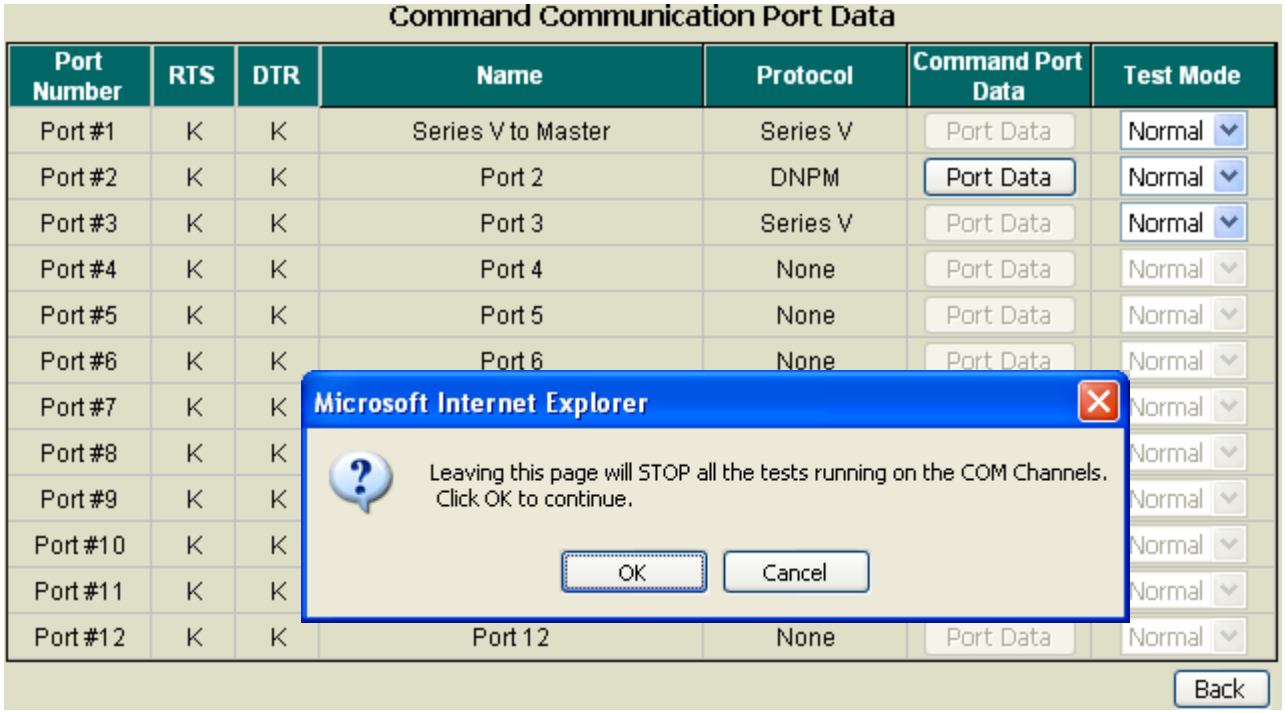
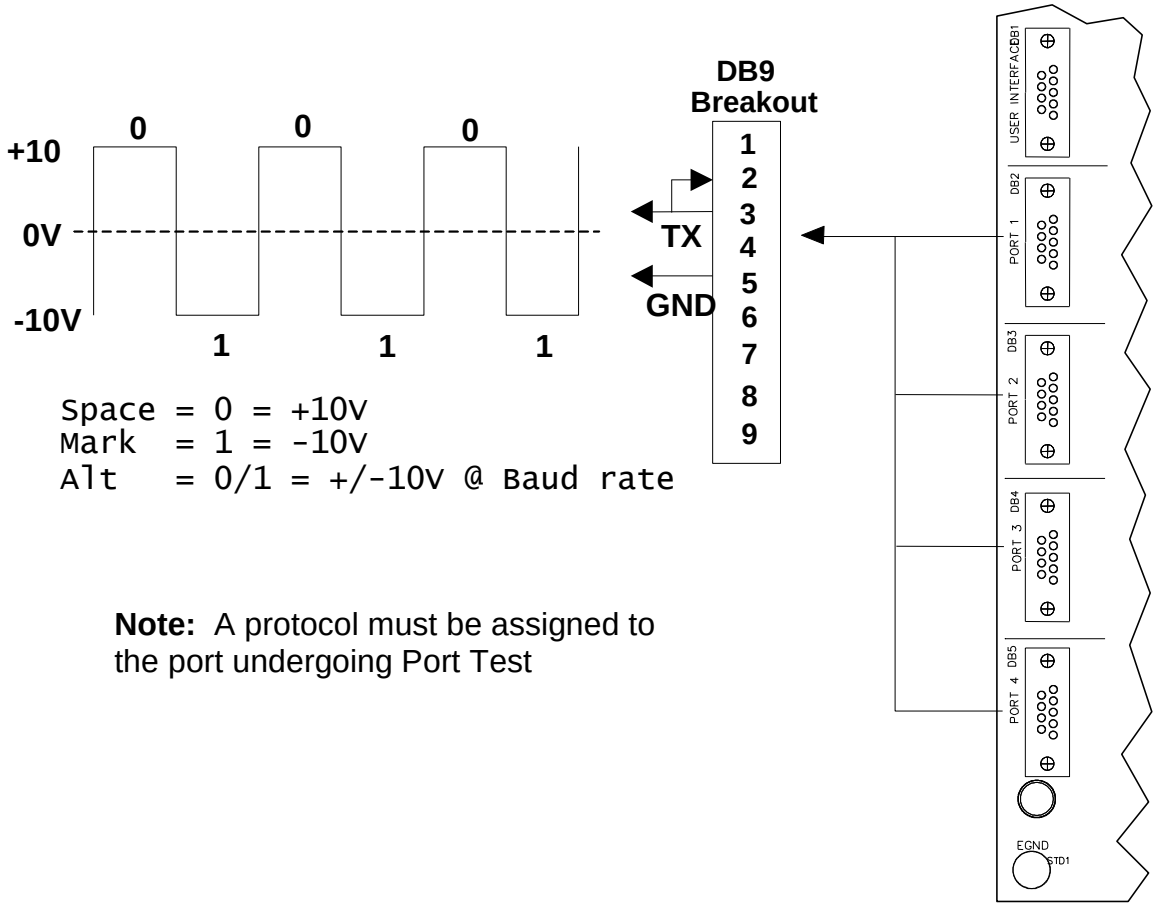


Figure 3-4 Comm Port Test



Note: A protocol must be assigned to the port undergoing Port Test

3.4 Analog Output Calibration

Refer to Table 3-1 for the following discussion.

The analog output boards can be calibrated using a firmware feature built into the AO XT. This calibration mode is selected using pencil switch S1 on the AO XT. One or more precision (±.1% or better) load resistors are required to calibrate current mode AO XTs, as listed below:

Output range	Load Resistor
4-20mA	250W
10-50mA	100W
0-1mA	5kW

Table 3-1 AO XT SW-1 Positions

SW-1			Resulting Function	
1	**2**	**3**		
Off	Off	Off	Ramp	Fast
Off	Off	On	Test	Slow
Off	On	Off	Hi	
Off	On	On	Lo	
On	X	X	Normal	

The procedure for calibrating an AO XT is as follows:

1. If the AO XT is one of the current mode versions listed above, connect the appropriate precision load resistor across the outputs (TB1, TB2, TB3, and TB4, terminals 1 and 3).
2. Verify that the +24VDC field power supply is connected to TB5-1 (+) and TB5-2 (-) and is energized.
3. Select the test mode by setting position 1 of the switch to OFF.
4. Select the high/low test by setting position 2 to ON.
5. Select the low output state by setting position 3 to ON. This will cause a value equivalent to 0% of full scale to be output to all four channels on the XT.
6. Connect the DVM across each channel in turn and adjust its output to the correct 0% of full-scale value using potentiometers R18, R20, R22, and R24 for channels 1 through 4 respectively. The correct minimum value depends on the output range of the AO XT as summarized in the Table 3-2.
7. Select the high output state by setting position 3 of S1 to OFF.
8. Adjust each channel output to the correct 100% of full-scale output value. The potentiometers used for the adjustment and the value of the output depend on the output range of the AO XT, as summarized in Table 3-3 (the potentiometers are listed for channels 1 through 4, respectively).
9. Repeat steps 3-5 as required to obtain settings that are within the ±0.1% rating for the AO XT.
10. Reset S1 to Normal operating mode.

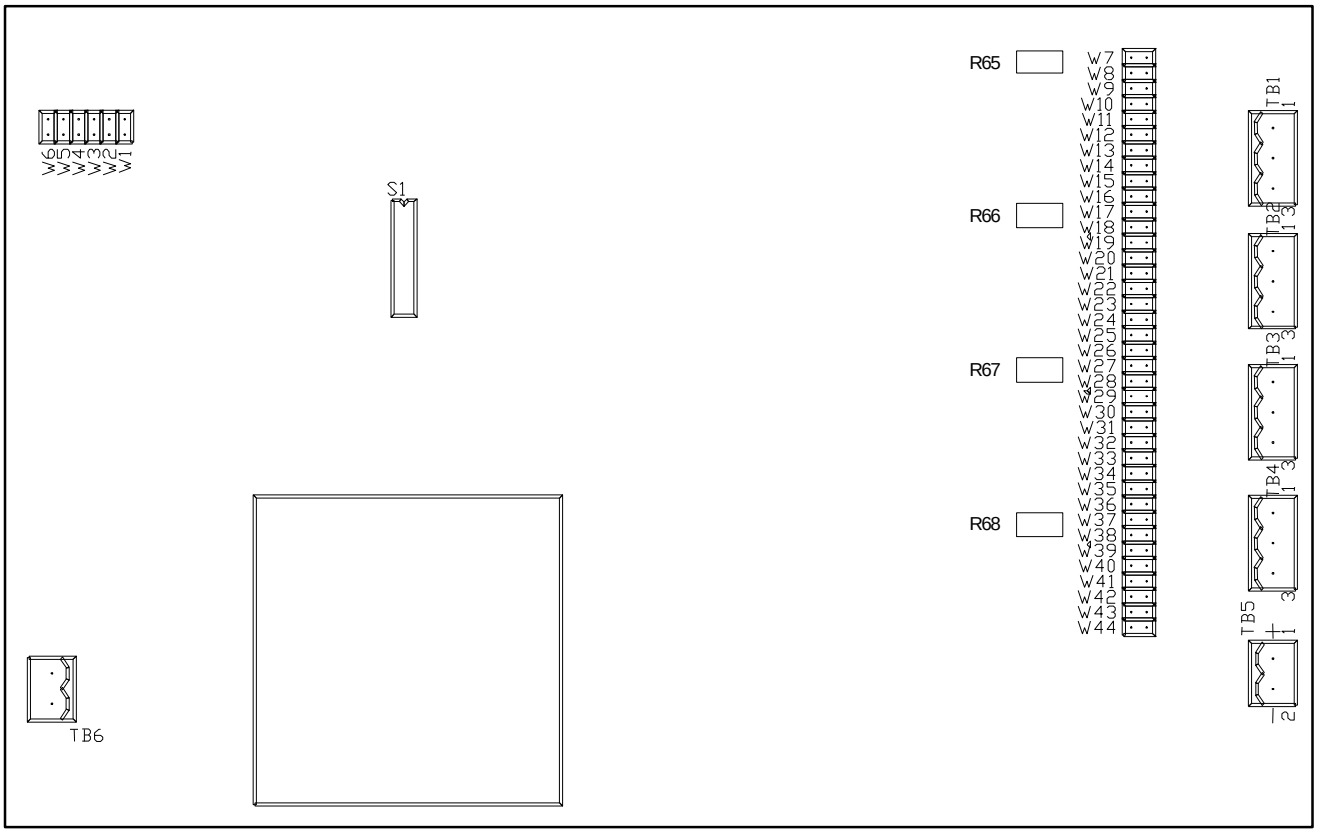
Table 3-2 AO XT Output Range Settings

OUTPUT RANGE 0%	SETTING
4-20mA	1.0 VDC (4.0mA)
10-50mA	1.0 VDC (10.0 mA)
0-1mA	0.0 VDC (0.0 mA)
±10V	-10.0 VDC
±5V	-5.0 VDC

Table 3-3 AO XT Output Range Adjustments

Output Range	100% Setting	Adjustments
4-20mA	5.0 VDC (20mA)	R17, R19, R21, R23
10-50mA	5.0 VDC (50mA)	R17, R19, R21, R23
0-1mA	5.0VDC (1.0mA)	R17, R19, R21, R23
±10V	+10.0 VDC	R65, R66, R67, R68
±5V	+5.0 VDC	R65, R66, R67, R68

Figure 3-5 AO XT Board Layout



3.5 Troubleshooting

This section includes a brief guide to troubleshooting some of the more common problems that could occur in the SAGE 2400. If you are troubleshooting to the component level, the use of the Theory of Operation chapter and the drawings in the SAGE 2000 manual will be helpful.

Caution: Do not insert or remove PC cards from the Baseboard or disconnect the ribbon cables to the XTs unless the power supply has been turned off.

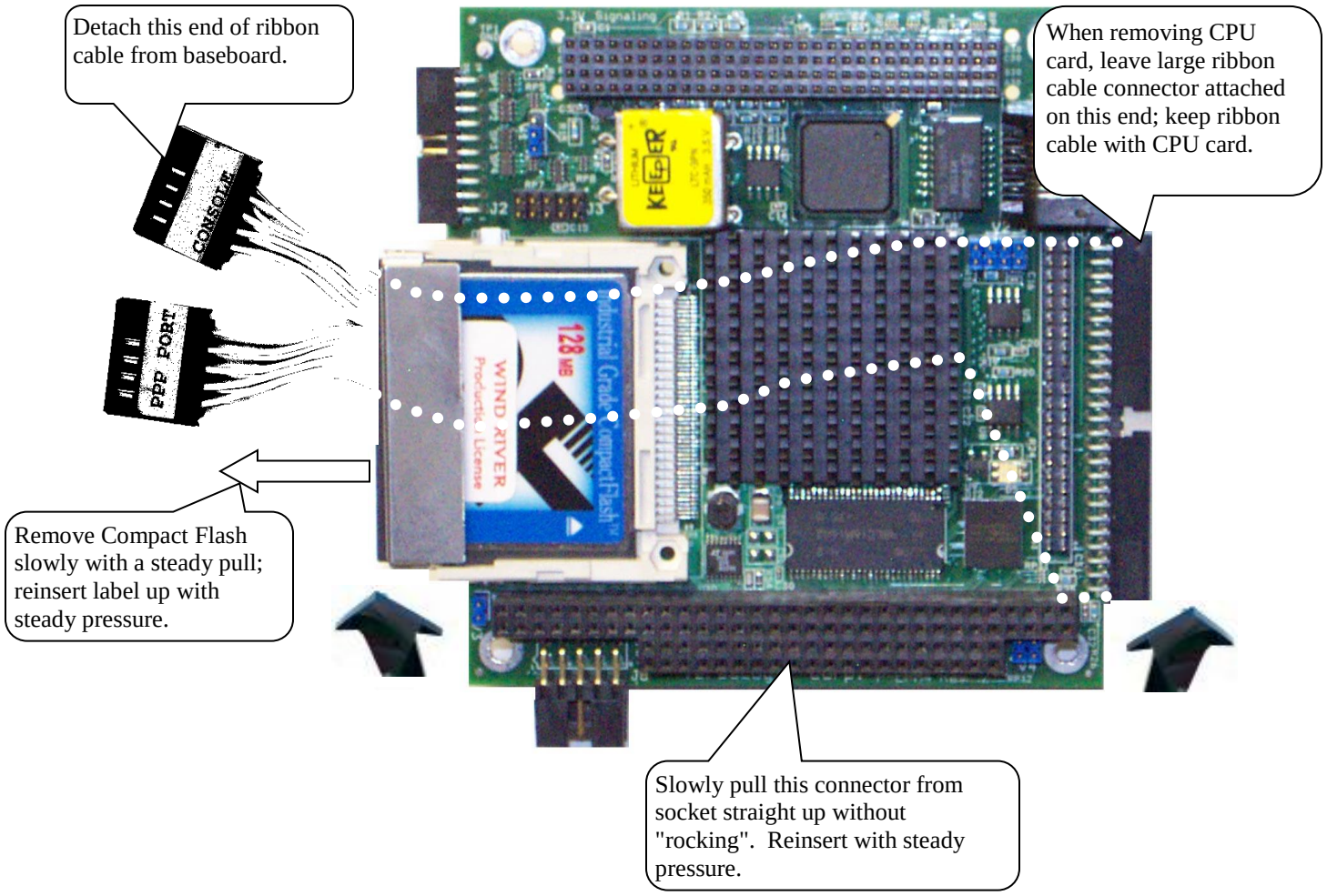
3.5.1 Removing PC/104 CPU Card or Compact Flash

If you determine that the PC/104 CPU card or the Compact Flash must be removed or reinserted for any reason, follow the directions below.

Note: Ensure power is OFF before disconnecting anything on the RTU.

Note: For those Compact Flashes that have a retaining clip, remove the clip carefully because if the clip springs out of its holder, it can damage small parts on the CPU card.

Figure 3-6 PC/104 CPU Card with Ribbon Cable & Compact Flash



3.5.2 Visual Inspection

A visual inspection of the equipment is often a good place to start the troubleshooting process. Look for frayed or loose connections, blown fuses, and any indications of damage or excessive wear. Check that switches and jumpers are in the right position and that input power is being supplied to the RTU and the XTs attached to it. Verify that the LEDs are providing expected indications compared to the present status conditions.

3.5.3 Data Display

You can use the Data Display Menu to monitor the operation of input and output devices. Most I/O XTs include LEDs to indicate the state of the equipment attached to them. The Data Display can be compared to the LEDs as a means of status verification.

3.5.4 LED Indicators on Baseboard

Refer to Figure 3-8 for the location of LEDs, Test Points, and adjustments on the Baseboard, and to Figure 3-7 for the location of LEDs on the C3438 Communications Expansion Card. The SAGE 2400 has been designed with an ample number of LEDs to provide the operator an indication of the activities being performed by the RTU.

Power

The power LED (DS52) is illuminated and Baseboard power is provided when SW2 is on.

Local/Remote (Relay Power)

When SW1 is in the remote position LED DS54 is illuminated. The RTU relays are thereby powered. This feature is utilized in the local mode during maintenance to prevent relays from unintentional operation of controls. Control is restored to the RTU by moving the switch to the remote position. The RTU can sense the position of the switch and store the information as a database point.

Communication

Each of the RS-232 communications ports, both on the baseboard and on the C3438, is annunciated by 5 LEDs as noted in Table 3-4 and Figure 3-7.

Table 3-4 Communication LEDs

Signal	Baseboard					C3438 Communications Expansion Card							
	UIF	CH-1	CH-2	CH-3	CH-4	CH-1	CH-2	CH-3	CH-4	CH-5	CH-6	CH-7	CH-8
Tx	DS19	DS24	DS29	DS34	DS39	DS5	DS10	DS15	DS20	DS25	DS30	DS35	DS40
CTS	DS20	DS25	DS30	DS35	DS40	DS4	DS9	DS14	DS19	DS24	DS29	DS34	DS39
RTS	DS21	DS26	DS31	DS36	DS41	DS3	DS8	DS13	DS18	DS23	DS28	DS33	DS38
Rx	DS22	DS27	DS32	DS37	DS42	DS2	DS7	DS12	DS17	DS22	DS27	DS32	DS37
DCD	DS23	DS28	DS33	DS38	DS43	DS1	DS6	DS11	DS16	DS21	DS26	DS31	DS36

PCI

DS17 and DS18 indicate the status of the two high-speed pulse counter input circuits.

SBO/DO

Eight LEDs (DS44 through 51) illuminate when each of the SBO/DO relays have been energized. Only one LED will be illuminated at a time for the SBO operations.

Status

LEDs DS1 through DS16 indicate activity on the 16 Baseboard status input points.

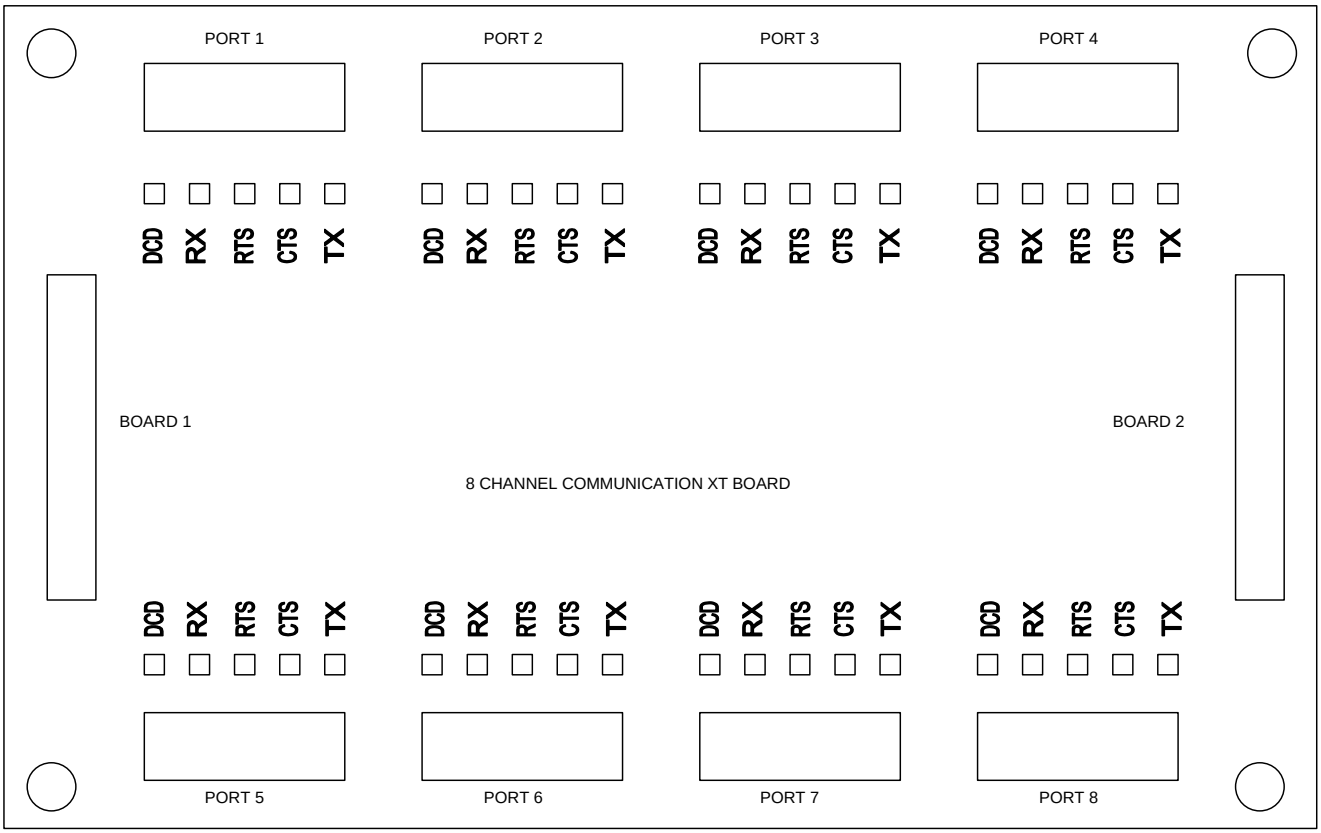
Reset

DS53 is illuminated anytime a reset operation is in progress on the Baseboard.

Alarm 1 & 2

DS55 and DS56 indicate the active state of Alarm Relay 1 and Alarm Relay 2 respectively. These auxiliary devices are programmable by Schneider Electric for special firmware application.

Figure 3-7 C3438 Board Layout



3.5.5 Test Points

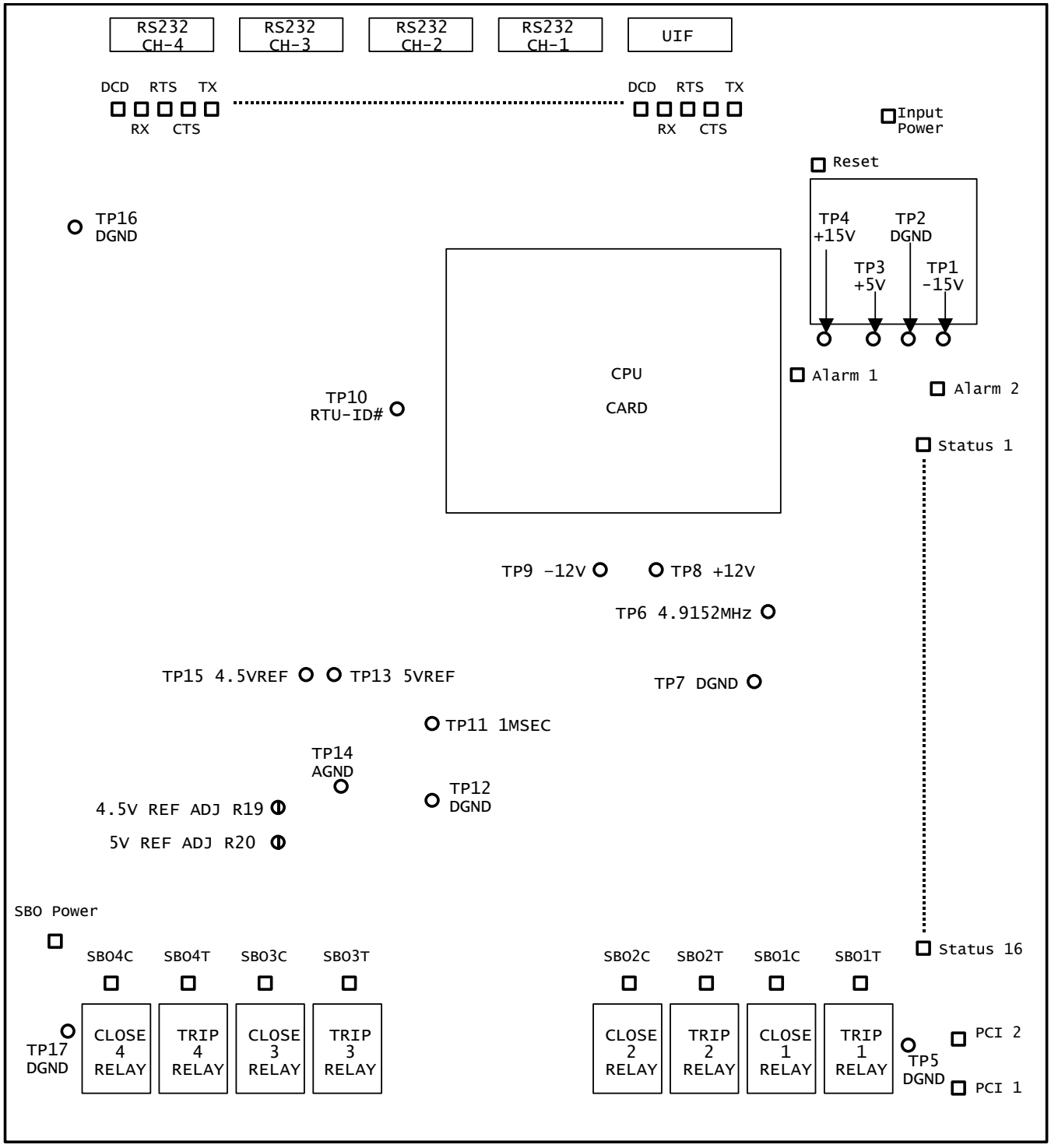
The following test points are included on the SAGE 2000 baseboard:

Table 3-5 Test Points

Testpoint	Signal
TP1	-15 Volts
TP2	DGND
TP3	+5 Volts
TP4	+15 Volts
TP5	DGND
TP6	4.9152 MHz
TP7	DGND
TP8	+12 Volt
TP9	-12 Volts
TP10	* RTU-ID
TP11	1 msec
TP12	DGND
TP13	5 Volt-Ref
TP14	AGND
TP15	4.5 Volt-Ref
TP16	DGND
TP17	DGND

* This signal is asserted as a low pulse whenever any I/O is accessed on the baseboard.

Figure 3-8 Baseboard LED, Test Point, & Adjustment Map



3.6 Jumper Positions, Baseboard

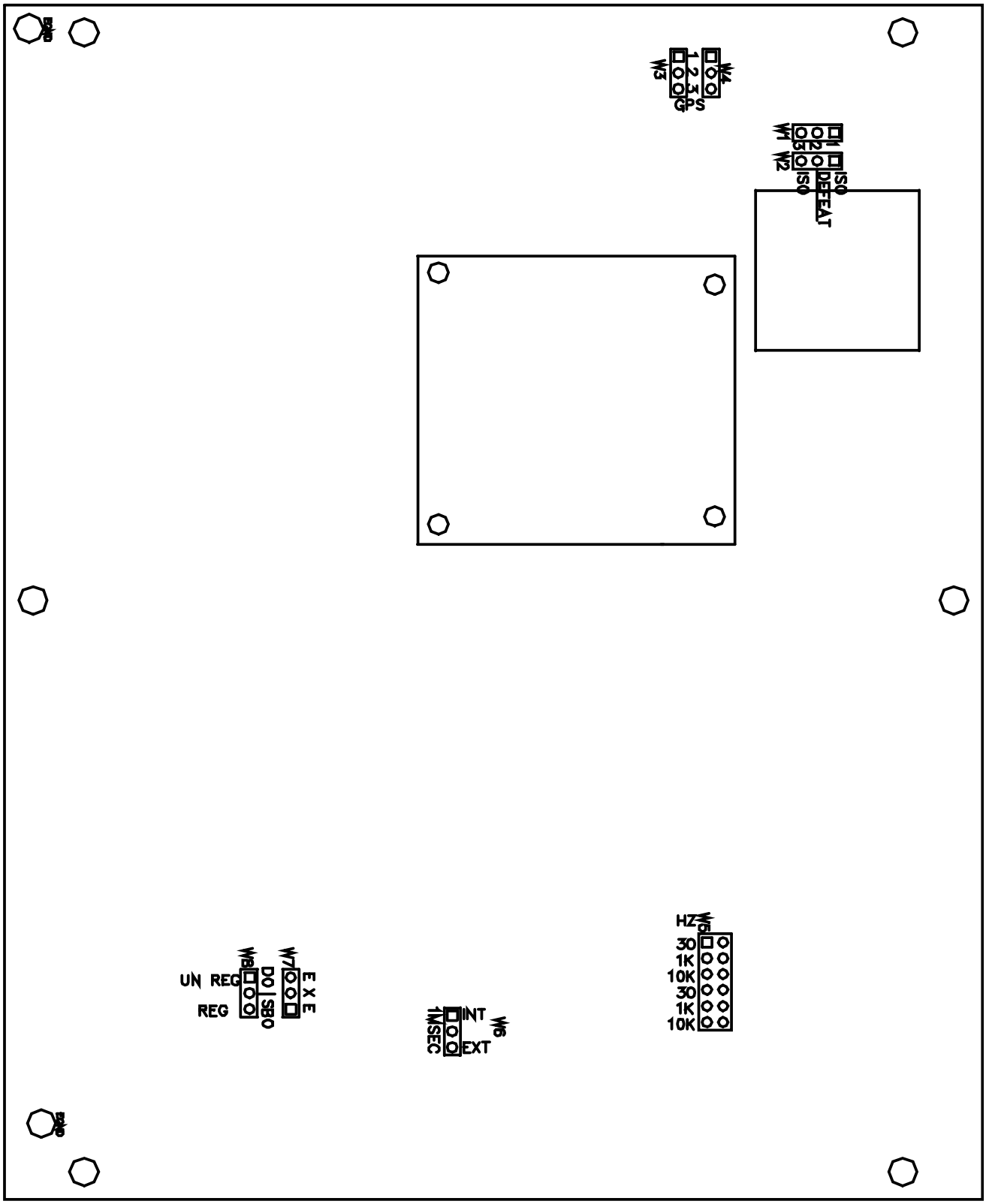
The factory test Baseboard jumpers are positioned as noted in Table 3-6 and Figure 3-9. This may not agree with the configuration required for proper operation of your RTU. Determine the setup for your RTU by checking the function column in the table. For a detailed view of the SAGE 2400 baseboard, please see the SAGE 2000 Operation & Maintenance manual (C3400-AAA-00002).

Table 3-6 Jumper Positions, Baseboard

Jumper	Name	Pins	Normal	Function	Sheet
W1	ISO DEFEAT	1-2	IN	Power Isolation Defeat	6 OF 6
W1	ISO	2-3		Power Isolation	6 OF 6
W2	ISO DEFEAT	1-2	IN	Power Isolation Defeat	6 OF 6
W2	ISO	2-3		Power Isolation	6 OF 6
W3	RS-232	1-2	IN (Always)	IN (Always)	1 OF 6
W3		2-3			1 OF 6
W4	RS-232	1-2	IN (Always)	IN (Always)	1 OF 6
W4		2-3			1 OF 6
W5	30	1-2		PCI Filter IN = 30Hz ch 1	4 OF 6
W5	1K	3-4		PCI Filter IN = 1kHz ch 1	4 OF 6
W5	10K	5-6	IN	PCI Filter IN = 10kHz ch 1	4 OF 6
W5	30	7-8		PCI Filter IN = 30Hz ch 2	4 OF 6
W5	1K	9-10		PCI Filter IN = 1kHz ch 2	4 OF 6
W5	10K	11-12	IN	PCI Filter IN = 10kHz ch 2	4 OF 6
W6	INT	1-2	IN	1-2 IN = internal 1 msec signal	3 OF 6
W6	EXT	2-3		2-3 IN = external 1 msec signal	3 OF 6
W7	SBO	1-2	IN	1-2 IN = SBO	5 OF 6
W7	DO	2-3		2-3 IN = DO	5 OF 6
W8	UNREG	1-2		1-2 IN = DO	6 OF 6
W8	REG	2-3	IN	2-3 IN = SBO	6 OF 6

Note: Some installations may require that the RTU ground "float" with respect to earth ground. You may float the RTU with respect to earth ground by placing W1 & W2 in the ISO position. However, there are disadvantages to floating the RTU. If you use ISO position, you cannot use DOs and you cannot read VBAT in analog references (the RTU will not be able to read the input voltage supply).

Figure 3-9 SAGE 2400 Baseboard Jumpers



3.7 Jumper Positions & Test Points, C3437 PC/104 Communications Card

Please see the CPU Manual to set jumpers correctly.

Figure 3-10 Jumper Positions & Test Points, C3437 PC/104 Communications Card

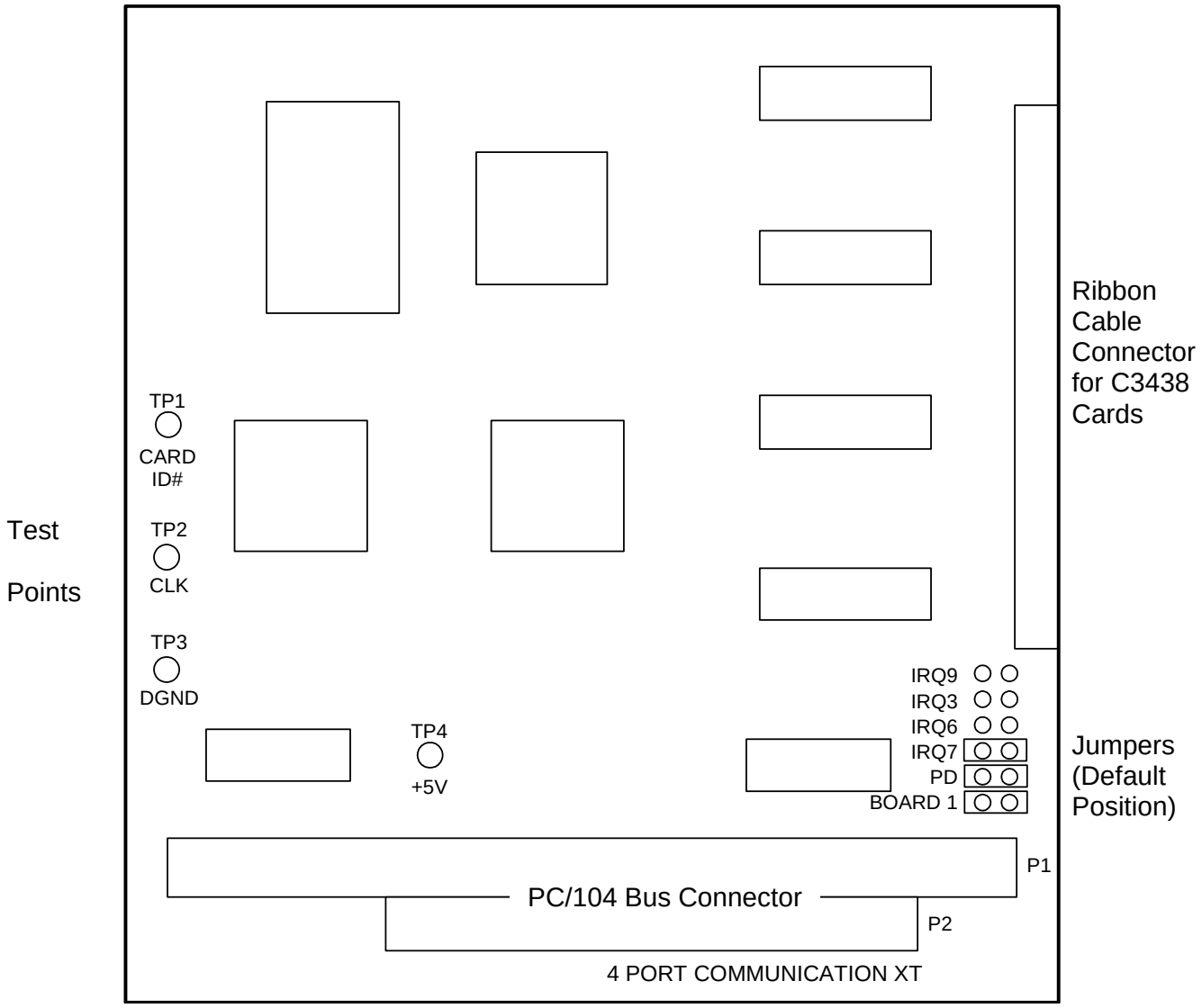


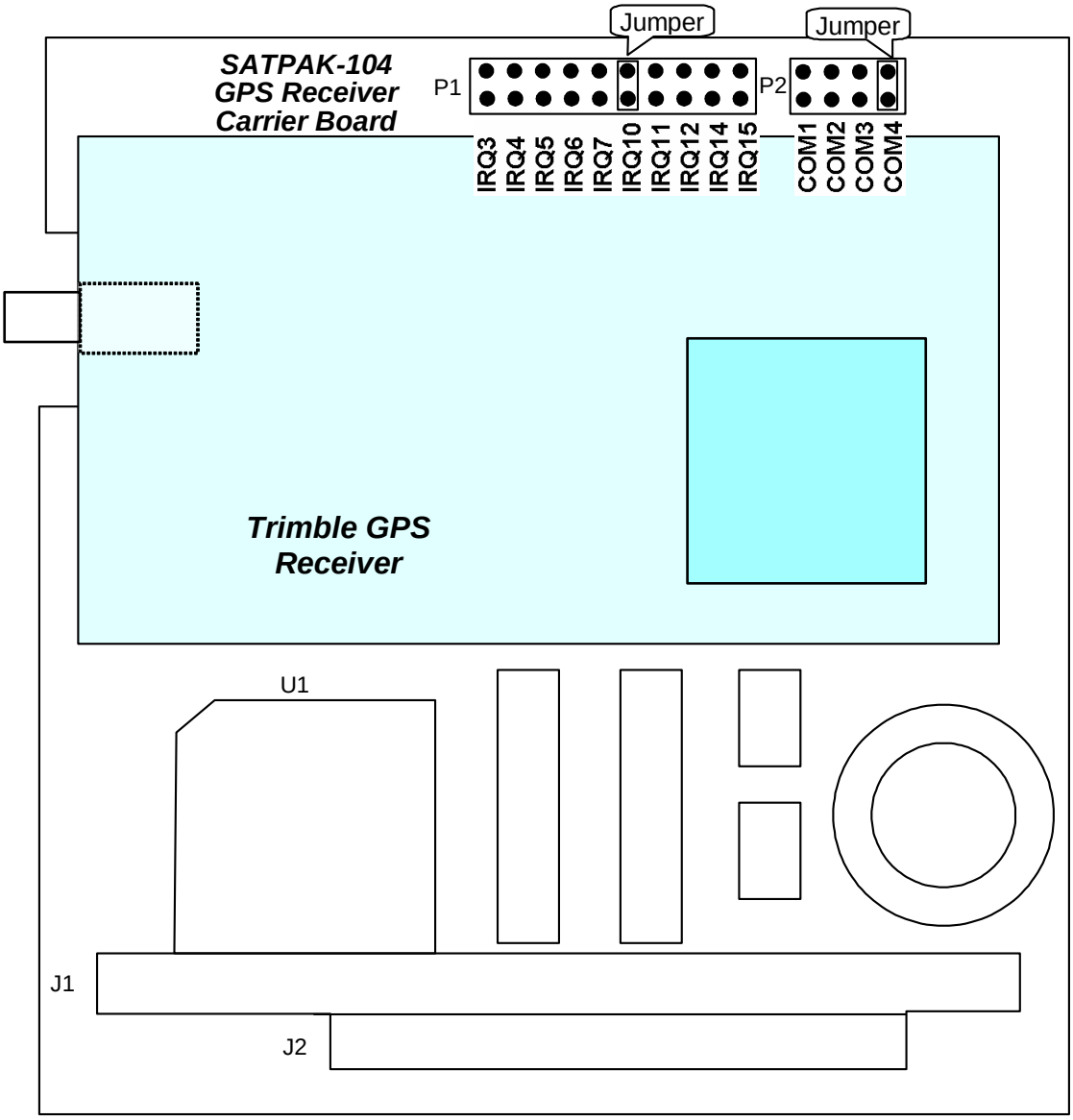
Table 3-7 Jumper Chart

JUMPER	SECTION	PIN	DEFAULT INSTALL	DESCRIPTION
W2	IRQ9	1–2		INTERRUPT 9
	IRQ3	3–4		INTERRUPT 3
	IRQ6	5–6		SHARED INTERRUPT 6
	IRQ7	7–8	IN	INTERRUPT 7
	PD	9–10	IN	PULLDOWN RESISTOR
	BOARD 1	11–12	IN	BOARD 1 SELECT

Jumper Positions, C3461 PC/104 GPS Card

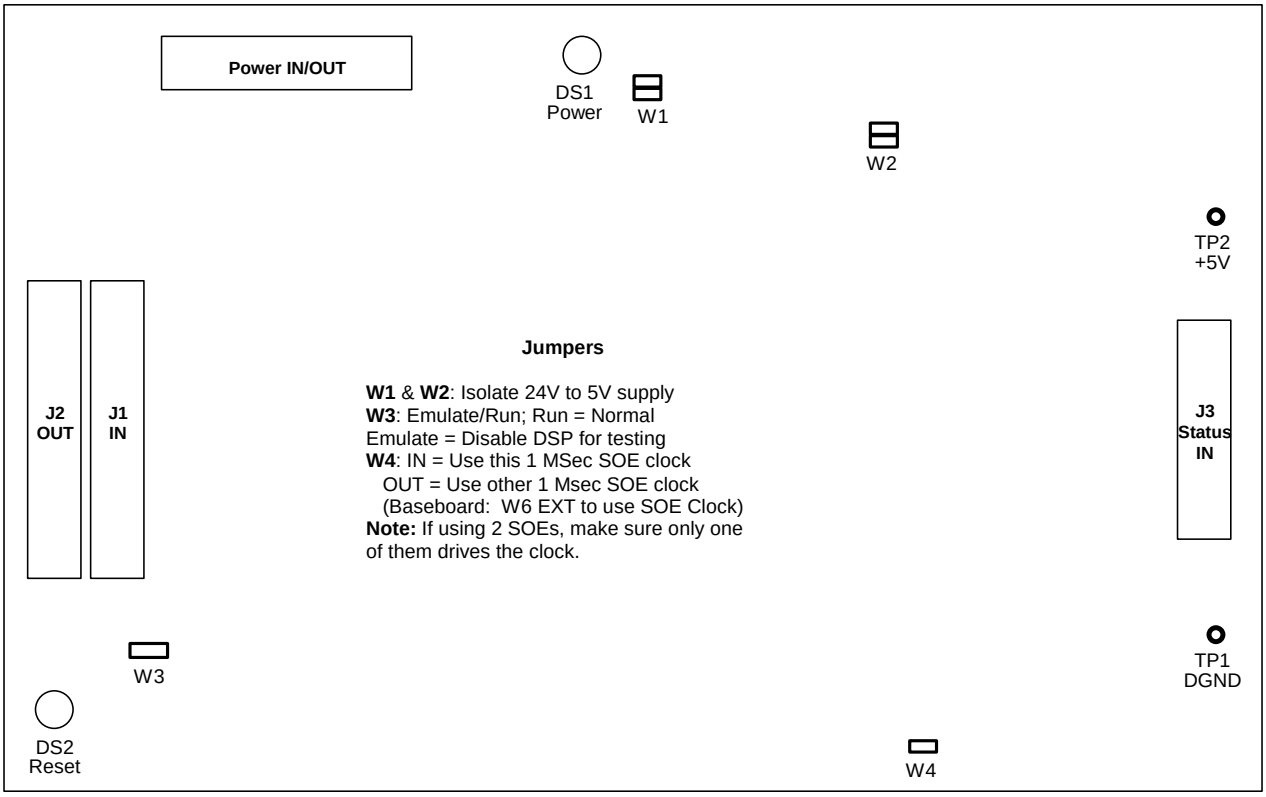
Please see the CPU Manual to set jumpers correctly.

Figure 3-11 Default Jumper Positions, C3461 PC/104 GPS Card



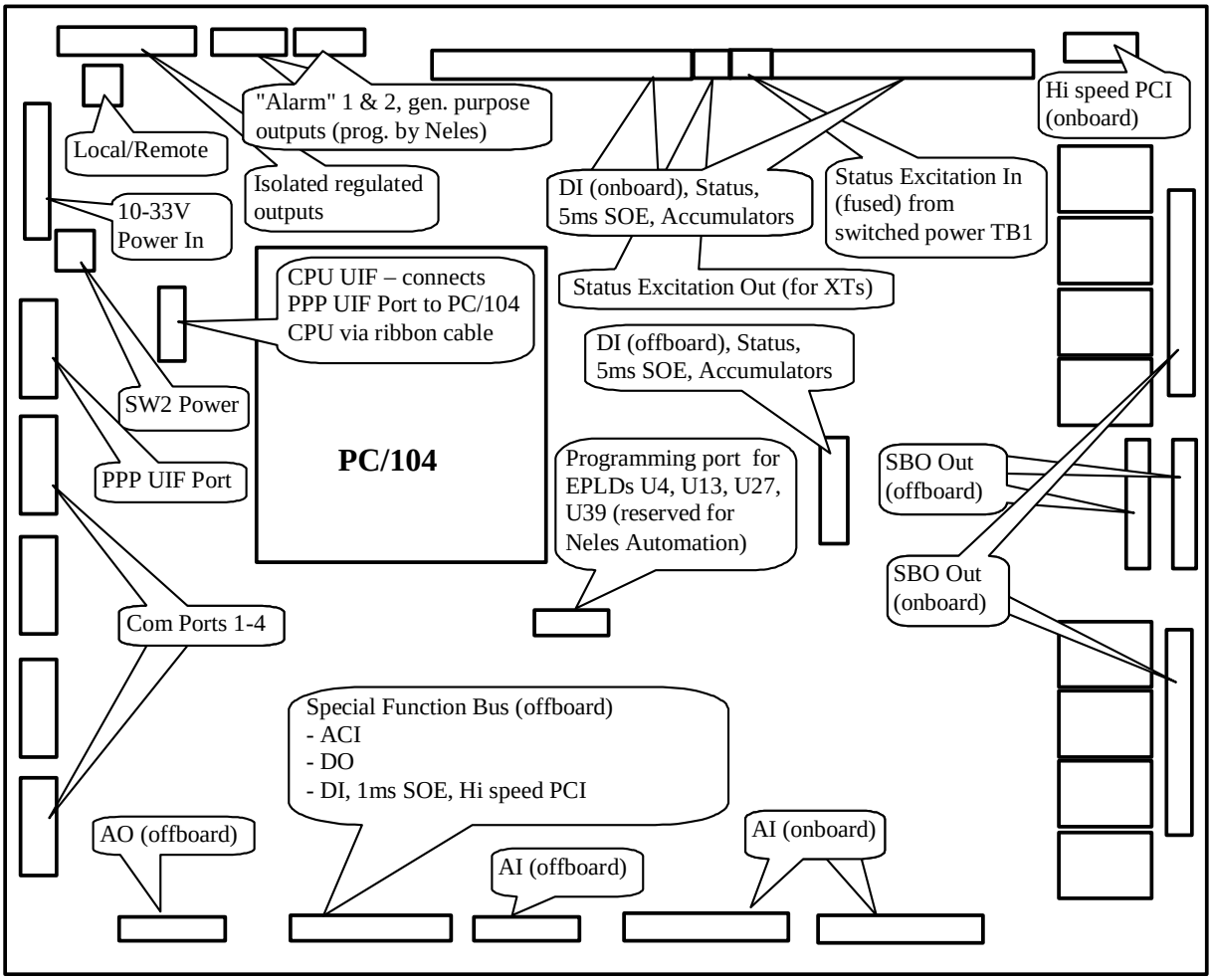
3.8 1 MSEC SOE Test Points, Jumpers & LEDs

Figure 3-12 1 MSEC SOE Test Points, Jumpers & LEDs



3.9 I/O Locations & Functions

Figure 3-13 I/O Locations & Functions



4 Theory of Operation

This section provides detailed technical design information on the SAGE 2400 and its various external modules, including design of the firmware and hardware. It is intended for use by those who wish to perform component-level troubleshooting and repair on the modules. This section is based on the simplified block diagrams included with the text. The schematic drawings and printed circuit assembly drawings contained in the SAGE 2000 manual can be used for a more detailed study.

4.1 Basic Architecture

The SAGE 2400 is composed of a Baseboard and a PC/104 CPU daughter board. Each unit performs a specific part of the functions necessary for operation as an intelligent remote terminal unit in a SCADA system. The Baseboard gathers data from the XTs and handles all communications with the Master Station(s). The PC/104 CPU maintains a central database containing all of the input/output data and issues various types of commands as they are received from the Master Station(s).

Wiring is brought onto the Baseboard and XTs through the use of terminal blocks. The XTs are connected to the Baseboard through ribbon cables. Each XT is designed to handle a certain input or output function. Each Baseboard and XT printed circuit assembly contains user terminations, transient protection, and any required input signal conditioning devices.

4.1.1 PC/104 Architecture

The open architecture of the PC/104 bus interface provides for expanded functions. You may add a PC/104-based GPS receiver and/or C3437/C3438 Communication cards that allow up to eight additional Comm ports.

The PC/104 architecture is a compact version of the IEEE P996 (PC and PC/AT) bus, optimized for the unique requirements of embedded systems applications. The PC/104 bus derives its name from the 104 signal contacts on the two bus connectors (64 pins on P1, plus 40 pins on P2). The main differences from the IEEE P996 are:

1. Reduced form-factor (3.550 x 3.775 inches)
2. Self-stacking, eliminating need for backplanes or card cages
3. Minimized component count and power consumption (typically 1-2 watts per module) and reduced bus drive requirement (typically 4 mA)

4.2 SAGE 2X00 Microprocessor Overview

Please refer to the CPU Manual

4.3 Hardware Design

4.3.1 PC/104 Bus Interface/Connector

The bus interface connector is compatible with the PC/104 Consortium specification.

Contact the Consortium at:

PC/104 Consortium
849 Independence Ave., Suite B
Mountain View, CA 94043
Phone: 650.903.8304
Fax: 650.967.0995
Email: info@pc104.org

The PC/104 standard is available on the web in downloadable PDF format at:

URL: http://www.pc104.org

4.3.2 C3437 PC/104 4-Port Communication XT

Each C3437 supports four external ports on a C3438 card. Up to eight ports are supported by using two C3437 PC/104 cards and one C3438 Port XT. The C3437 is connected by ribbon cable to the C3438.

P1 acts as the PC/104 interface. The card acts as an 8bit slave ISA card and as such only decodes the first nine addresses from the bus. Addresses SD15 - LA23 are in the connector but not brought out to the RTU.

The communication controller is a Zilog 85230. These devices have 4 byte TX FIFOs and 8 byte RX FIFOs.

Figure 4-1 C3437 Board Layout

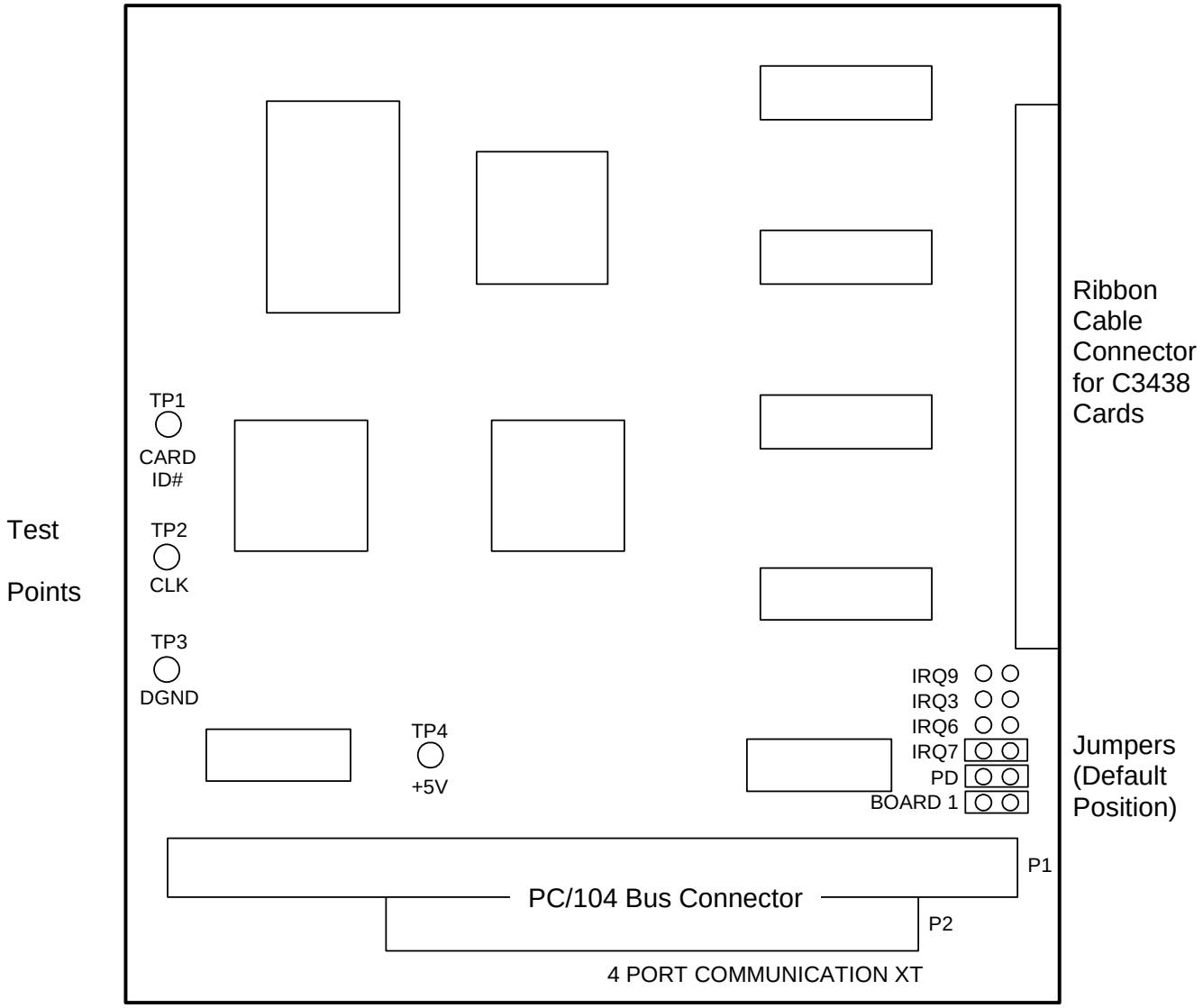


Table 4-1 Jumper Chart

JUMPER	SECTION	PIN	DEFAULT INSTALL	DESCRIPTION
W2	IRQ9	1–2		INTERRUPT 9
	IRQ3	3–4		INTERRUPT 3
	IRQ6	5–6		SHARED INTERRUPT 6
	IRQ7	7–8	IN	INTERRUPT 7
	PD	9–10	IN	PULLDOWN RESISTOR
	BOARD 1	11–12	IN	BOARD 1 SELECT

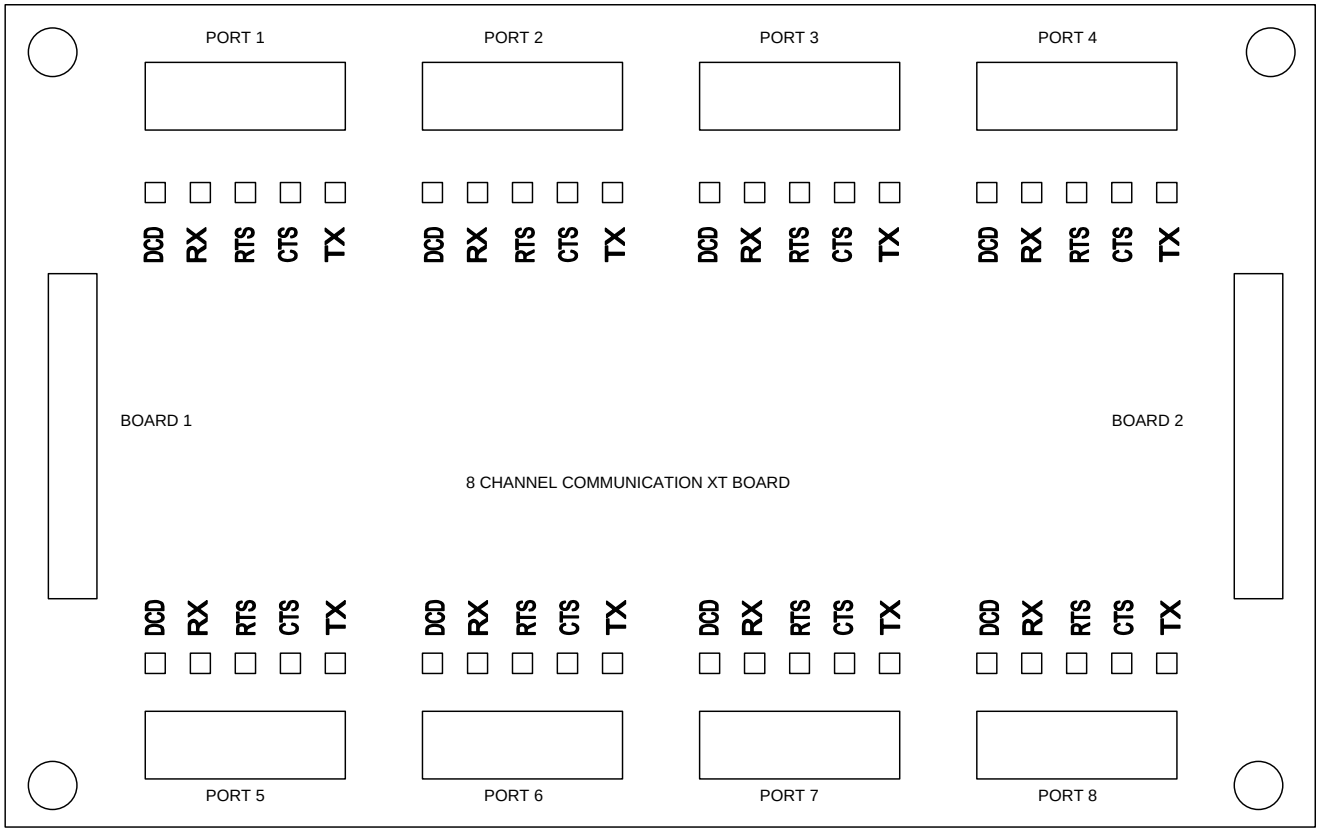
Table 4-2 I/O Port Addresses for the 4-Channel C3437 Communications Card

Port (hex)	ACRONYM	DEFINITON	READ/WRITE
180-183	CS-COM1&2	85230 Ports	READ & WRITE
184-187	CS-COM3&4	85230 Ports	READ & WRITE
188-18B	CS-COM5&6	85230 Ports	READ & WRITE
18C-18F	CS-COM7&8	85230 Ports	READ & WRITE

4.3.3 C3438 8-Channel Communication XT

Each port on the C3438 has its own RS232 driver. Each of the eight ports are identical and each can receive both transmit and receive clocks.

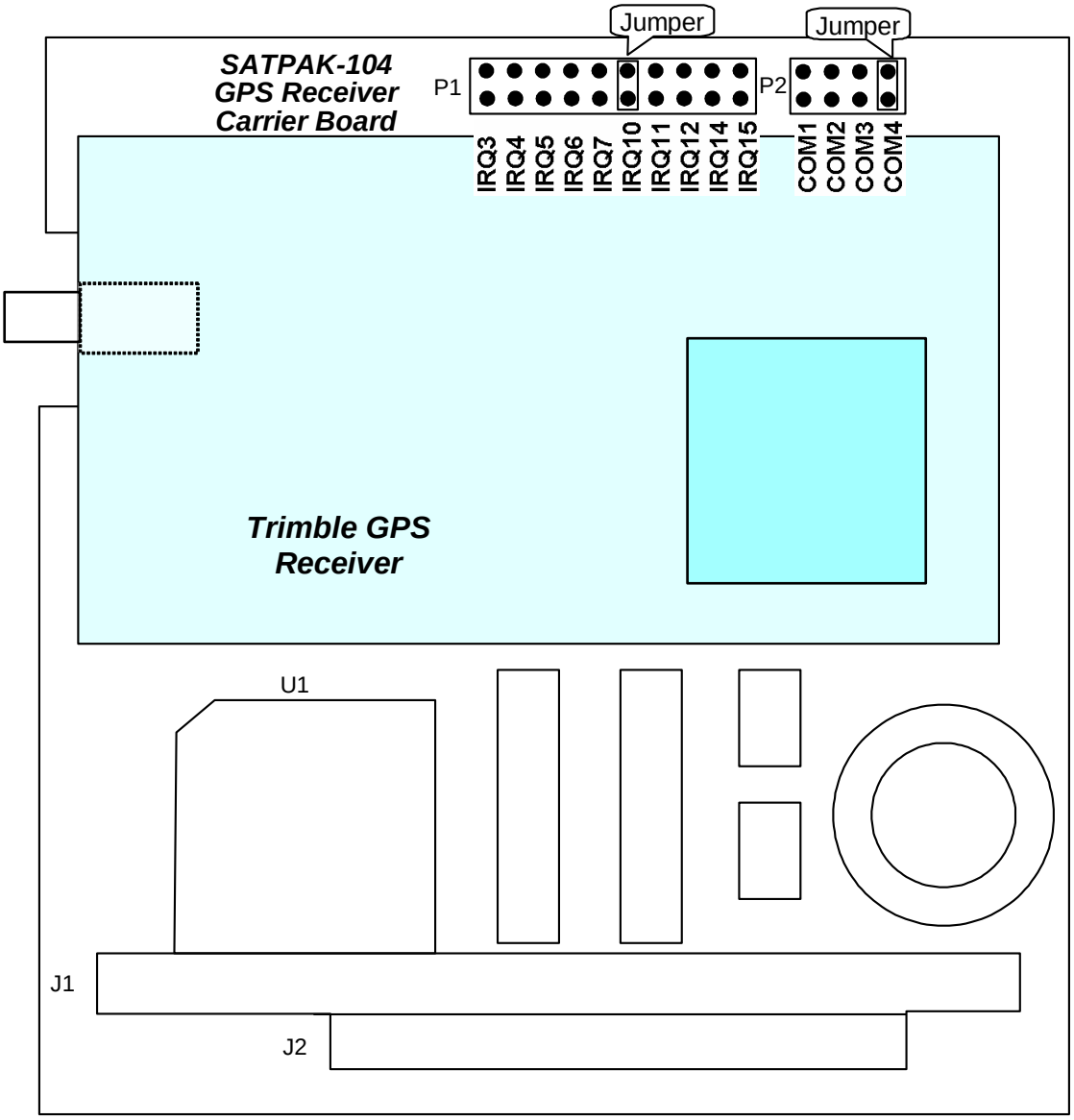
Figure 4-2 C3438 Board Layout



4.3.4 C3461 PC/104 Trimble GPS Receiver

The C3461 PC/104 Trimble GPS receiver consists of two boards; a PC/104 carrier card (SATPAK-104), with a Trimble GPS receiver riding piggy-back. See Figure 4-3.

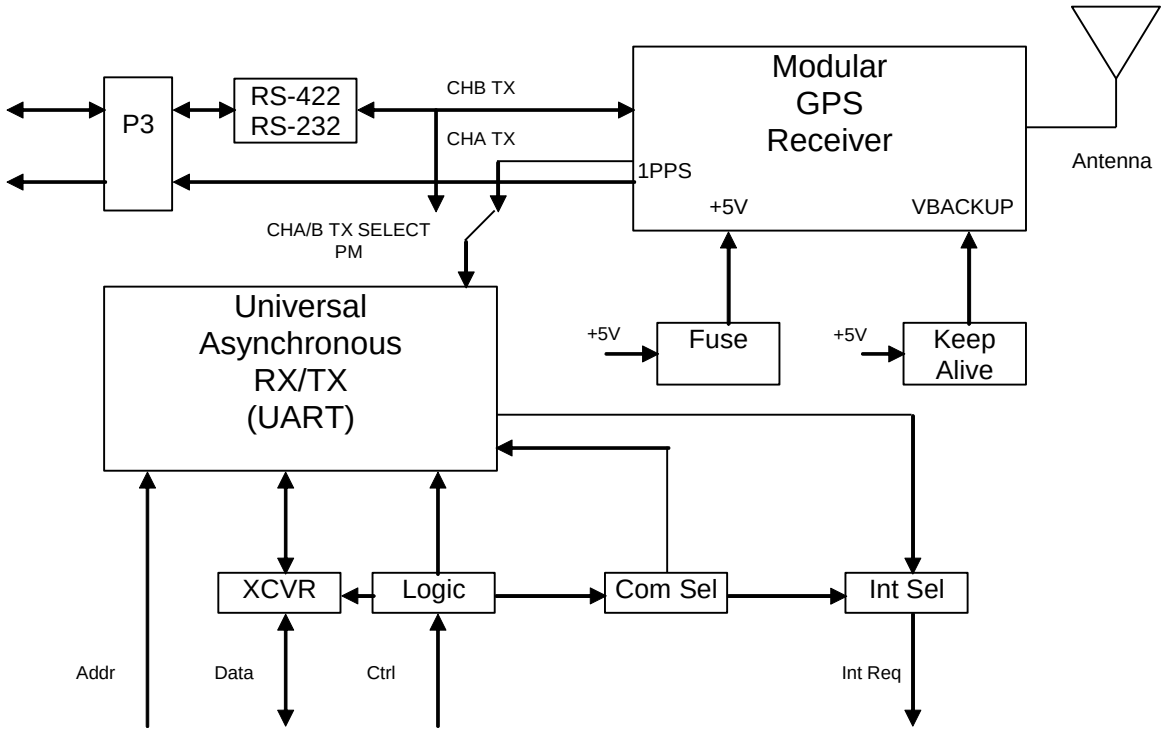
Figure 4-3 C3461 Board Layout (Default Jumper Positions)



The SATPAK-104 communicates with the GPS receiver through a 16550 universal asynchronous receiver/transmitter (UART). The UART converts the serial TTL data required by the GPS receiver to parallel data required by the PC/l04 protocol. Simple push-on jumpers are used to configure the SATPAK-104 for standard input/output base addresses (COMI, COM2, COM3, COM4) and any of the available bus interrupt lines (IRQ3-IRQ7, IRQl0-1RQl2, IRQ14, or IRQ15). The J2 pass-through connector option must be installed to access interrupt request signals IRQ10-IRQ12, IRQl4, and IRQl5. Custom programmable logic is available if the user must decode base addresses other than those supported by the standard serial communication addresses. The SATPAK-104 also provides signal level conditioning for RTCM-104 serial differential correction signals (RS232 or RS422), and a large value l Farad capacitor to maintain the almanac, ephemeris, and real-time clock of the GPS receiver after power is removed. The GPS receiver is protected with a thermally resettable fuse in line with the +5V power to the GPS receiver. The IPPS signal from the GPS receiver is available on connector P3 located on the SATPAK-104.

The overall block diagram for the PC/104-Trimble receiver combination is shown in Figure 4-4.

Figure 4-4 GPS Receiver Block Diagram



4.3.5 Baseboard Precision Oscillator

The SOE XT (C3235) provides accuracies of 1ppm if they are required. The 1msec timing pulse is the basic time keeping signal in the SAGE 2400. If no C3235 SOE cards are present, the processor will sense that there is no 1msec clock and will thereupon provide the source for the 1msec clock.

4.3.6 I/O Select Expansion

PLD devices provide addressing of 4 additional functions (I/O mapped) (Table 4-3) beyond the EPLD capabilities.

Table 4-3 SFB and Analog Input I/O Addressing

PLD	Name	Function
U27	SFBSEL#	Special Function Bus Select
	SFBADDR#	Special Function Bus Address Enable
	AICHNL#	Analog Input Channel Address Enable
U13	CS-ADC#	Analog/Digital Converter Select

SFBSEL#
The address (0-7)through which data is written to or read from the SFB XT or AO XT which has been selected.

SFBADDR#
Data written to this address is latched in the SFB address latch (U37). This is used to select whether a SFB XT or an AO XT will be addressed, which XT will be addressed, and which address on the XT will be written or read.

AICHNL#

AICHNL# originates in EPLD U27; it enables address lines A-A0 through A-A4 in the Analog EPLD U13. These address lines determine the analog channel fed to the A/D converter.

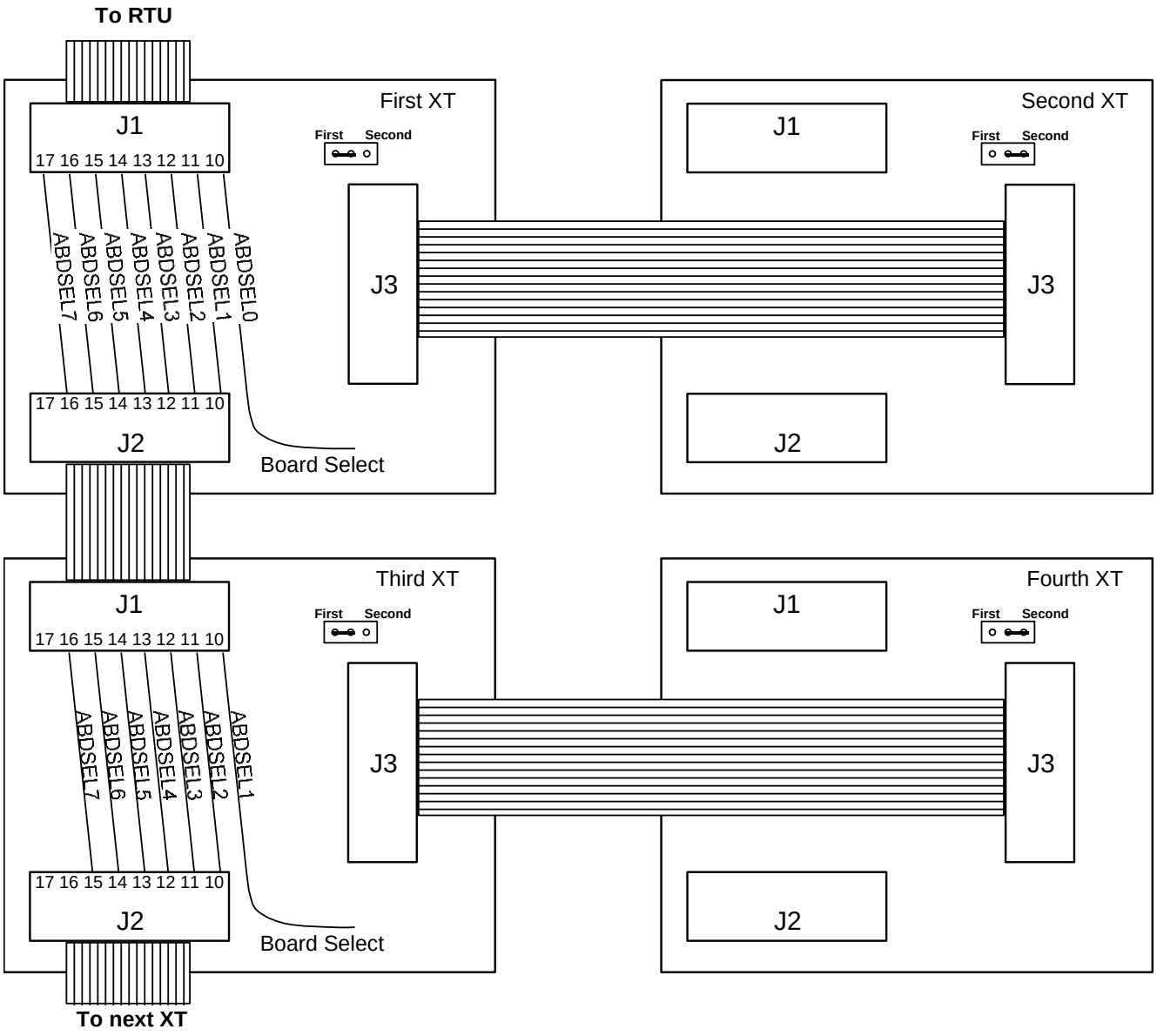
CS-ADC#
CS-ADC# originates in the Analog EPLD U13; it selects the A/D converter to begin a conversion.

4.3.7 Expansion (XT) Architecture

Figure 4-5 shows the cable routing for half panel size XTs. The XT address structure is contained in the combination of the cable routing and the position of the XT in the daisy-chain. The XTs on the left side of the figure are the first half addresses while the right side are the second half. FIRST and SECOND jumpers on the XTs are set accordingly. The exception to this configuration is the C3233 SBO XT. In this case the J3 connector of the first XT is cabled to J1 of the second XT.

The XT board select signals (e.g., ABDSEL0) are rotated on the XT boards as illustrated in Figure 4-5. Each XT board is selected by the signal that arrives at J1, pin 10. The board select signal that appears on J1, pin 11 exits on J2, pin 10 to be received at J1, pin 10 of the next XT in line. Each additional select signal is transposed in the same manner.

Figure 4-5 XT Cable Connections



4.3.8 Special Function Bus

The Special Function Bus is used to expand the I/O capabilities of the SAGE 2400. The SFB signals appear on J6 and J7. J6 is used to support the analog output XT (C1009). The pin assignments for J7 are noted in Table 4-4.

Table 4-4 Special Function Bus Pin Assignments

Pin	Signal	Pin	Signal	Pin	Signal
1	DGND	13	B-S-A2	25	B-SFBSEL2
2	+5V	14	B-S-A3	26	B-SFBSEL3
3	+15V	15	SFB0	27	B-SFBSEL4
4	RTU-RESET#	16	SFB1	28	B-SFBSEL5
5	BWR/RD#	17	SFB2	29	B-SFBSEL6
6	EXT-1MSEC	18	SFB3	30	B-SFBSEL7
7	BWR-RD#	19	SFB4	31	-15V
8	No Connection	20	SFB5	32	+5V
9	BSTB	21	SFB6	33	DGND
10	DGND	22	SFB7	34	DGND
11	B-S-A0	23	B-SFBSEL0		
12	B-S-A1	24	B-SFBSEL1		

RTU-RESET#
A signal provided by the Baseboard. It is asserted whenever the RTU is being reset, which includes periods when the 5V supply is outside of acceptable thresholds. This signal is active when it is low and is pulled low on each XT.

BWR/RD#
A signal provided by the Baseboard to specify whether data is being written to or read from the XT. A high logic state (+5V) indicates a write from the Baseboard to an XT. This line must be high if data is to be written to the XT, or low if data is to be read. This signal should be left in the low (read) state when unused.

EXT-1MSEC
A precision 1kHz frequency clock driven by the Baseboard or the SOE XB if installed. This will allow the operation of SOE XTs with perfect synchronization to the Baseboard and other SOE XTs.

BSTB
It is provided primarily to support the Analog Output bus, which is a subset of the Special Function Bus. It is asserted high after all addresses are selected on the AO bus.

B-S-A0 to B-S-A3
Address lines, used for decoding and selecting one of 16 addresses on a single XT board. Each address may be used for read or write.

SFB0-SFB7
Bi-directional data lines for reading or writing.

B-SFBSEL0 to B-SFBSEL7
Are used to select one of 8 XTs. A maximum of 8 full size XTs of any mixture of types can be attached to the special function bus. Note that certain types of XTs, such as the Digital Output, use jumpers to allow the use of a pair of half size XTs in place of a full point count XT.

4.3.9 Power Input

The SAGE 2400 Baseboard accepts +10 to +33VDC as a power input. Additional inputs of 48VDC and 129VDC may be used with a DC/DC converter. 120VAC or 240VAC may be used with the appropriate supply/charger.

Terminal block input TB1-3 is used for the +10 to +33VDC input. The return is connected to TB1-1 or TB1-2. The input is surge protected by varistors RV4-5 and reverse voltage protected by diode CR65. Over-voltage protection is provided by zener CR111. SW2 controls the power on-off while an LED (DS52) indicates the presence of power to the Baseboard.

In minimum configurations, the entire RTU may be operated from this single power source, including analog current loops and digital input loops. The +10 to +33VDC is used to energize relays. The analog and logic voltages needed for the operation of the rest of the system are derived from +10 to +33VDC by regulators that generate the ±5V volts and ±12 volts. Zener diodes (CR19, 20, 60, 62) protect the output lines from over-voltage.

4.3.10 Local/Remote Switch

The Baseboard SW1 allows you to disable all relay coil excitation power. LED (DS54) is off and power to the SBO and DO relays is disabled in the local position. Pins 5, 6 and 7 of TB1 provide a form C contact for LOCAL/REMOTE selection. The contacts allow connection of the LOCAL/REMOTE switch to a Status Input point.

See the Installation chapter for additional information. The Baseboard SBO relay coils are disabled during power-up reset. This is to prevent any premature SBO relay excitation until the microprocessor has stabilized after any reset or power-up operation.

4.4 Communication Ports

The SAGE 2400 baseboard has 4 RS-232 serial communication ports plus one RS-232 User Interface port. The ports are accessed through 9 pin female connectors. Each pin has electrical surge protection. The combined data rate for all four ports is 100K baud. Baud rates are individually selected by port for rates between 300 and 9600 baud. The UIF is dedicated at 38,400 baud.

4.5 Analog Inputs

The analog input subsystem used in the SAGE 2400 employs firmware to perform a ratiometric conversion. The subsystem can be calibrated while the RTU is running and is easier to calibrate than other systems. Refer to Figure 4-6.

4.5.1 Interface and Protection

Each analog input point is provided with a pair of screw terminals. A grounded screw terminal is supplied for each pair of input points for drain wire (shield) connections.

The normal connection allows for voltage or current inputs from transmitters that are excited by the signal they read. Surge protection is provided by a MOV device, a high-voltage ceramic capacitor, and an RC network that also serves as a lowpass filter for normal mode signals. This arrangement meets the IEEE surge withstand capability specification and in addition provides insurance against surges induced by lightning. No fuses are used in the analog input circuits.

4.5.2 Internal Voltage Levels

The output from the sample/hold circuit is attenuated by R116 and R117; this gives nominal attenuation of 0.95. This attenuation allows the ADC to read greater than 5V, by 1/0.95, or about 5.3%. The auto-span firmware scales the internal 5V reference point to read 3900 counts.

4.5.3 Internal References

The SAGE 2400 has 6 internal points (Analog Reference Voltages) two of which (ground reference and 5V reference) are used for auto-nulling and autoscaling. All six values are available to be mapped as regular database points. These points are as follows:

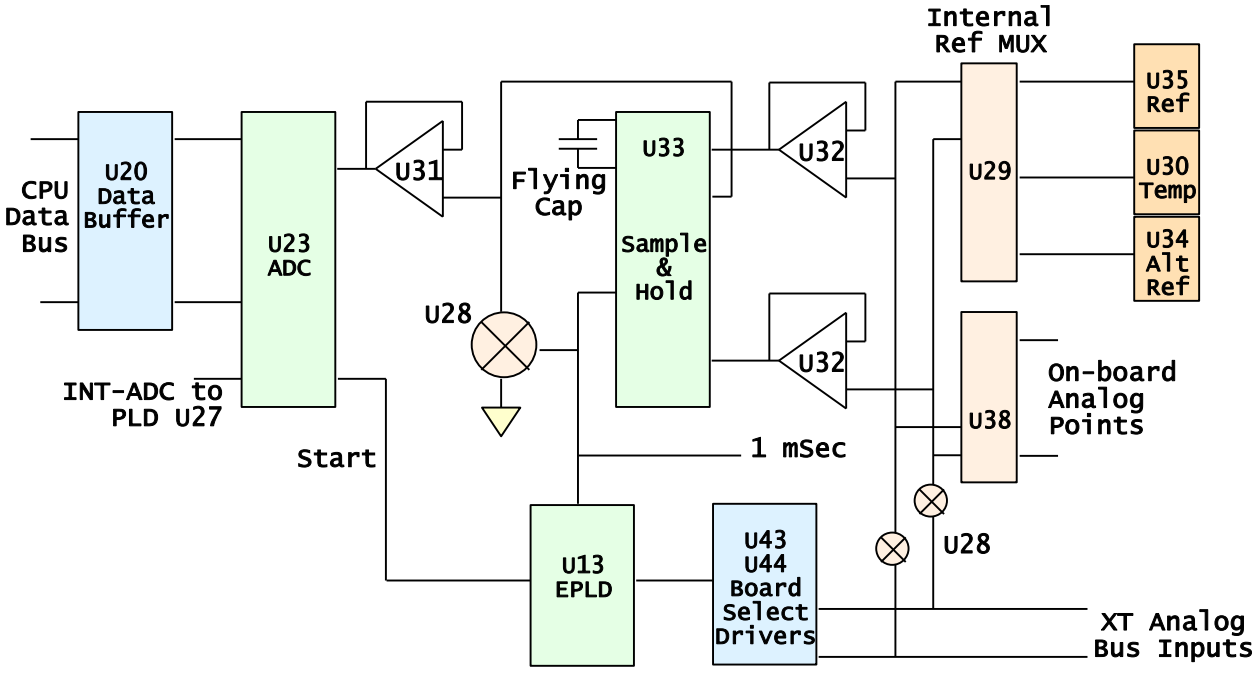
11. Ground reference
12. 5V reference
13. +4.5V reference
14. -4.5V reference
15. Temperature
16. Baseboard DC Input Voltage

The ground reference point is used by the auto-nulling firmware to correct for DC offset within the sample/hold circuit and the ADC. Firmware reads the ground reference point periodically, stores the reading and subtracts this stored value from all points before any further processing.

The 5V reference is used by the auto-scaling firmware to correct for span drift with time and temperature. The 5V reference point is read periodically and the reading is used to scale all other points (except for the ground reference) such that all readings are a ratio (point reading/5V reading). The 5V reference is stable with time and temperature. The 4.5V reference point is used mainly as a linearity check for the system; it is not integral to system operation. It should be noted that the 4.5V reference is derived from a second, independent, 5V reference chip.

The 4.5V reference output is buffered with an opamp, so connection of a multimeter without high impedance inputs should not affect the voltage being adjusted. The -4.5V reference is created from the +4.5V reference by changing the sign and treating it as just another multiplexer point. This allows the analog inputs to be monitored for differential linearity errors.

Figure 4-6 Analog Input Block Diagram



The temperature sensor has a basic slope of about 10 mV per degree C. The voltage is fed directly into the A/D to calibrate it for temperature drift. Temperature is also output as a reference point and may be sent to the Master. See Table 4-5 for temperature/voltage relationship.

Note: The voltage readings in Table 4-5 are idealized. The IC is an Analog Devices TMP36 with a typical accuracy over the temperature range of ±2% and a typical linearity of ±0.5°C. The temperature range is –40°C to +125°C

Table 4-5 Reference Temperatures

C	K	F	Volts
+28	301	82.4	0.780
+26	299	78.8	0.760
+24	297	75.2	0.740
+22	295	71.6	0.720
+20	293	68.0	0.700
+18	291	64.4	0.680
+85	358	185.4	1.350
0	273	32.0	0.500
–40	233	–40	0.100

The baseboard DC Input reference voltage point is connected to the Baseboard input power and is attenuated to fit within the 5 volt span.

4.5.4 Multiplexer and Sample/Hold Circuit

The SAGE 2400 can address up to fourteen AI XTs. Each XT has two differential multiplexers to select eight channels each. The eight Baseboard analog inputs have their own multiplexer (U36) while the references have a separate multiplexer (U29). The analog subsystem can thereby handle a maximum of 232 analog inputs (14x16+8). See Table 4-6 for point inputs. The AI XT board multiplexers are not routed through the Baseboard internal points mux. All Baseboard and XT multiplexer outputs are bused together.

The analog input muxes feature break before make switching. Each channel has a 1µF capacitor (for low pass filtration) directly connected to the mux inputs. If the muxes didn't have break before make switching, then small but noticeable charge transfers would occur between channels when switching. This would reduce the analog accuracy.

The sample and hold (S/H) device (U33) used by the SAGE 2400 has the added feature of performing level shifting at unity gain. The sample and hold consists of a differential 4-channel mux, a polypropylene capacitor (C55), and three op-amps (U32A and B, and U31B) configured as unity gain buffers. The op-amps connected to the analog bus present a high impedance to the bus and a low impedance to channel 1 of the mux. The polypropylene capacitor is connected to the output terminals of the mux. Input 2 of the sample and hold mux is used as an output going to the A/D converter. The + terminal is buffered by the third amplifier and the – terminal is tied to analog ground at the ADC.

The S/H mux channel one is addressed when a new sample is desired. This allows the input buffer amps to charge the capacitor (C55) to the input voltage. Channel two is then addressed to connect the capacitor to the ADC. This is effectively a flying-capacitor multiplexer.

The time required to charge the capacitor voltage to within 1/2 LSB of the final value is 11RC time constants for this system. The resistance in the calculation is the resistance in series with the outputs of the input buffer amps to limit the maximum current flow. The S/H mux has a high internal resistance that limits the peak current to a reasonable level. The 0.33 µF hold capacitor then provides a worst case settling time of 180 µsec.

Table 4-6 Analog Input Point Assignment

Address (hex)	Connection
0-F	No connection
10-17	Internal points
18-1F	Baseboard points
20-3F	32ch XT #1
40-5F	32ch XT #2
60-7F	32ch XT #3
80-9F	32ch XT #4
A0-BF	32ch XT #5
C0-DF	32ch XT #6
E0-FF	32ch XT #7

A polypropylene capacitor is essential because the sample and hold capacitor must provide very low dielectric absorption (the tendency for a capacitor to remember the last charge) and low leakage. Channels 3 and 4 of the S/H mux are unused.

The analog switch connected to the S/H output buffer amp input is controlled by the 1MSEC signal. The 1MSEC has a 50% duty cycle. This switch shorts out any stray capacitance in the S/H mux output circuit when the S/H is sampling a new value. This is necessary because the hold capacitor is discharged slightly when the S/H goes into the hold state.

The ADC1251 has tri-state outputs, but IC U20 is installed in series with the ADC on the data bus. This has been done to minimize the activity on the data bus at the ADC pins. The addition of U20 results in a significant reduction in analog noise as seen by the ADC.

4.5.5 Event Timing

The operation of the analog input subsystem is fairly simple, but a few details should be pointed out. First, the converter generates an interrupt when a conversion is complete. Second is that the convert-complete interrupt is the SAGE 2400s basic firmware timing signal (at 1kHz). The baseboard 1kHz clock is configured to start the ADC conversion and it is the completion of the conversion that interrupts the processor to inform it that, not only is there data to read, but also that a new millisecond has occurred.

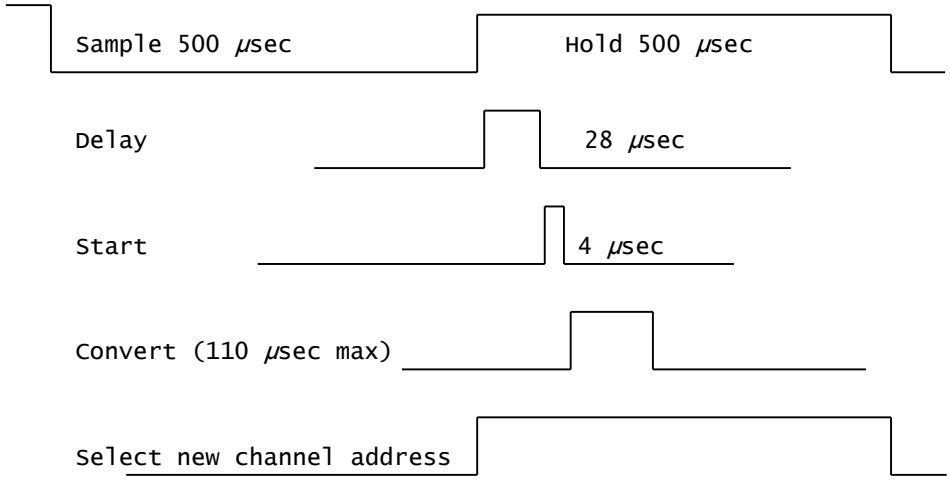
The ADC start-convert signal is generated by a timer in EPLD (U13) 28 µsec after the S/H is switched to the "hold" state. The sequence of events for making a single reading is as follows:

1. This step is joined in progress. The 1msec clock line is low for a 500 µsec period. The S/H is in sample mode, and the multiplexers (from previous commands) have the correct channel selected. There is adequate time for the multiplexers and S/H input amps and capacitor to track and settle to the new analog value.
2. The 1msec clock line goes high. This switches the S/H to the hold state, and starts the 28 µsec timer. The 28 µsec timer allows the S/H output opamp to settle to the new sampled value before the ADC starts.
3. After the 28 µsec timer times out, the rising edge of the 4 µsec start-pulse triggers the ADC to begin conversion. The ADC takes approximately 110 µsec to perform the conversion. The S/H is still in the "hold" state, and is required to droop less than 0.5 LSB during the conversion period.
4. The ADC interrupts the processor, indicating it has completed the conversion. The data is read by the processor, and a new channel address is written to the multiplexers. Both reading the data and writing the new channel number can be performed at a leisurely pace if desired, as ample time exists. The S/H is still in the "hold" state.
5. The 1msec clock line goes low. This sets the S/H in the sample mode. The new channel number for the multiplexers is already written, so the S/H starts tracking the new analog value at this time. This is the step that was joined in progress in step 1 above. If the new channel number is not yet

written, then the S/H will start to track the old analog point instead, until the new channel number is written.

The SAGE 2400 rejects 60Hz or 50Hz noise by adding an initial analog sample to another sample taken 540 degrees (1.5 cycles for 60Hz) or 180 degrees (0.5 cycles for 50Hz) later. The two samples are averaged. Because the two samples will always be of opposite polarity but equal in amplitude, any AC noise should cancel, therefore rejecting AC noise at the power line frequency or any odd multiple.

Figure 4-7 ADC Timing



Rather than sampling a single point, waiting for 25 or 10msec and sampling it again, the points are converted in groups of 25 or 10, twice in a row. For example, with 60Hz rejection, points 1 through 25 are converted in sequential milliseconds, and the values are temporarily stored. Immediately, points 1 through 25 are converted again, and the two values are averaged before saving in the database. The next group of 25 points is given similar treatment until all analog points are read. Conversions recommence at the beginning of each second. Conversions are performed on an unspecified point, typically ground, with no data being stored, to maintain 1kHz clock ticks between the last field point conversion and the start of a new second.

The analog multiplexer address is written to I/O address 105h. In terms of addressing, the analog input points exist as a contiguous block of 240 points justified to the end of a space of 256 points. The ground reference is addressed when performing dummy conversions to mark time.

4.5.6 Analog Input XT

Refer to the following schematic drawings located in the SAGE 2000 RTU Operation & Maintenance Manual (C3400-AAA-00002):

- C3140-002-Rev-X, Schematic LD Analog Input XT 16PT
- C3230-002-Rev-X, Schematic M/1C 16PT Analog-In XT
- C3430-002-Rev-X, Schematic S2K 16PT Analog In XT
- C3241-002-Rev-X, Schematic M/1C Analog Input Module

The Analog Input XTs are available as an 8 X 5 or an 19" rack mount board that contain terminations for 16 analog channel inputs. Fourteen 16 input XTs can be connected to provide 232 inputs including the 8 Baseboard inputs. Each 16 input XT is provided with an address jumper to select either the first or second 16 point board for each pair of boards.

All analog inputs are high impedance while their outputs are differential to match the circuits on the Baseboard. The multiplexer, buffer amplifiers and input protection circuits on the XTs are identical to those on the Baseboard.

The board select and channel select input signals enter the XT on J1. These board address lines are rotated on each XT. This allows the next board in the daisy chain to accept the correct address without requiring address select jumpers. These signals exit the board on J2. J3 is a half board output connector and allows a second C3230 board to be connected as a pair. Jumper W1 provides address selection for the "FIRST" or "SECOND" position.

The multiplexer switches both the positive and negative inputs to each channel to allow for differential inputs. Channel selection is decoded by U3 and U4. The 5VDC used for these digital circuits is generated by a regulator (VR1) from the +15V. This isolates the board from other digital supplies for additional noise immunity.

Each rail of the multiplexer outputs is buffered and then isolated from the analog bus by a switch. These switches are controlled by the SW signal that is active when the board is selected for the proper half determined by jumper J1.

4.6 AC Inputs

Please refer to the C3244 AC Analog Input Option Manual (C3244-AAA-00011) for ACI Theory.

4.7 Analog Output

4.7.1 Analog Output C1009 XT

Refer to drawing no. C1009-002-00000, Schematic D/A M/1E 4CH Analog Output, located in SAGE 2000 RTU Operation & Maintenance Manual.

The Analog Output External Termination (AO XT) board provides four independent analog output points. The Baseboard supports AO XTs but does not have built-in analog outputs. The XT board uses an 8741 microcontroller chip (U5) to interface to the SAGE 2400 Analog Output bus (J6). Serial data inputs are required by the four 12-bit digital to analog converter chips (U15, U16, U17, U18). The serial data from the 8741 microcomputer is opto-coupled to the DAC chips to isolate the field electronics from the digital bus interface.

The bus interface section of the board is designed to be driven from an external power supply independent of the supply for the output or field section of the board. Therefore, if the RTU power fails, the loop current or output voltage will be maintained at the last set value until power can be restored to the RTU. TB6 is the RTU power input and TB5 is the field power input point.

With component and jumper changes in the output section of the board, either current loop or voltage outputs are available. The current loops can be configured as sink or source drives and as either 4-20mA or 10-50mA loops. Refer to drawing C1009-000-X00XX for a list of these configuration variances along with a bill of materials. Each mode; voltage, current sink and current source, is represented by a separate schematic as listed in Table 4-7.

Table 4-7 Schematic/Variance Cross Reference

VAR CONFIGURATION	C1009-000-X00XX
Current sink 4-20 mA	-1XXXX
Current sink 10-50 mA	-2XXXX
Voltage out ±5V	-3XXXX
Voltage out ±10V	-4XXXX
Current source 4-20 mA	-5XXXX
Current source 10-50 mA	-6XXXX
Current source 0-1 mA	-7XXXX
Other Voltage/Current outputs available as a special request	

The SAGE 2400 can address up to three AO boards on the AO bus (J6) for a maximum of 12 DAC outputs. The first board in the chain will be address selected by installing jumpers W1 and W2. The AO XT board can receive 6 board selects and it takes two board selects to perform the reads and writes to the card. This means that a maximum of 3 cards of 4 AO points each can be configured into the RTU for a maximum of 12 AO points. Use W1 and W2 to select the first board.

When either address line DS1 or DS2 is low, the chip select line of the 8741 will be enabled. When DS1 is low and the DA-STB (Digital to Analog Strobe) line is low, the SAGE 2400 writes data and command words to the 8741 database buffer on D0 through D7. When DS2 is low and the DA-STB line is low, the SAGE 2400 reads data and status words from the data bus buffer. The S-A0 line is used by the SAGE 2400 to indicate whether the byte transfer is data or command.

The 8741 has two quasi bi-directional ports. Port 1 is on lines P10-P17 which are used to read switch S1 for test purposes. Port 2 is on lines P20-P27 which are used to transmit the buffered serial data line (IDATA) and the five control lines (ICLK and LD1 through LD4).

The 8741 can be reset by the SAGE 2400 via U7 (on the C1009), or by the Vcc power monitor U14 (also on the C1009). U14 will also disable the 6 serial lines until the Vcc line has stabilized. By way of the 8741 TEST0 input and opto coupler U27, the CPU can test the status of the field power and report this back to the SAGE 2400.

U8 through U13 are opto couplers used to isolate the digital half of the board from the analog out section by transferring the signals IDATA, ICLK, and /LD1 through /LD4.

U15 through U18 are precision 12-bit multiplying DACs designed for the serial interface. They are used with a precision, temperature stable DC reference VR2 in a unipolar mode. The serial data on IDATA is clocked into the device on the negative edge of ICLK. The serial data is then loaded in the converter on a per channel basis by /LD1 - /LD4.

The output of the converters is buffer amplified by U19, U20, U21, and U22. The feedback resistor of the amplifier is on the converter between pins 16 and 1. The voltage output of this first op amp is given as:

$$Vo = \frac{Vref \times DigitalCode}{4096}$$

Since Vref is ten volts, when a 12-bit digital code of all ones (4095) is output to the C1009 card, this output voltage will ideally be:

$$Vo = \frac{10 \times 4095}{4096} = 9.9976\ volts$$

For a binary code of zero, all bits zero, the voltage output will be 0 volts.

From this first voltage output with a range of 0 to 10 volts, the rest of the output circuitry is designed to be capable of being configured at the factory to be one of six variations. The variances consist of two current sink variances, two current source variances, and two voltage output variances. The two variances per each current output are controlled by a single resistor per channel. The two variances of voltage output depend on whether the output span is ±5 volts or ±10 volts, the choice being controlled by a fixed resistor and a potentiometer per channel. The variation between voltage or current output is more extensive and the circuit operation description follows.

4.7.2 Voltage Output

Since each of the four outputs is identical, output #1 with its circuitry connected to TB1 can be used as an example.

The two voltage output configurations ±5V and ±10V differ only in the gain of the second stage op-amp (U23). The first stage op-amp U19 provides the same span for each voltage out configuration. The second stage op-amp receives the 0 to 10V span output from the first stage op-amp, and by adding gain and offset, scales it for ±5V or ±10V operation. Fine offset adjustment is provided to correct for any offset error by biasing U23 with an adjustable reference from R18 centered around zero volts.

Each channel will reach its full scale positive value with a digital input of 4095 and reach its full scale minus value with a digital input of 0.

4.7.3 Current Sourcing

Since each of the four outputs is identical, output #1 connected to TB1 can be used as an example.

The two current output configurations 4 to 20mA and 10 to 50mA differ only in the value of R69 that is in the feed back loop of the second stage op-amp U23. The first stage op-amp U19 provides the same span for each current out configuration. The second stage op-amp U23 receives the 0 to 10V span output from the first stage op-amp U19 and provides current sourcing by way of Q4, a FET. Offset and span adjustment is provided by R19 and R30 respectively. Each channel will reach its full scale positive value with a digital input of 4095 and reach its full scale minus value with a digital input of 0.

4.7.4 Current Sinking

Since each of the four outputs are identical, output #1 connected to TB1 can be used as an example. The two current output configurations, 4 to 20mA and 10 to 50mA, differ only in the value of R69 that is in the feed back loop of the second stage op-amp U23. The first stage op-amp U19 provides the same span for each current configuration. The second stage op-amp U23 receives the 0 to 10V span output from the first stage op-amp U19 and provides current sourcing by way of Q3, a FET. Offset and span adjustment is provided by R19 and R30 respectively. Each channel will reach its full scale positive value with a digital input of 4095 and reach its full scale minus value with a digital input of 0.

4.7.5 Power

The AO board is designed to use two separate power inputs: TB6 is the input for the board's digital power (generally supplied from the same power source as the RTU), and TB5 Field Power is the input for the analog section of the board (generally supplied from an independent power source). If the RTU power fails, then the AO board would still have analog power so that the last analog values will be held at the output.

Input power at TB6 feeds a switching regulator which supplies all the board's digital circuits.

Input power at TB5 (Field Power) feeds a DC to DC power supply which supplies +/- 15V to the board's op-amps. Field Power is also routed to the board's output where, in combination with jumpers W9 through W44, the board may be configured for combinations of current sink, current source, voltage out, with various combinations of 0-1mA, 4-20mA, 10-50mA, 0-100mA, +/- 5V, +/- 10V outputs. All these choices must also have the proper resistor combination installed.

4.7.6 AO Self Test

S1, whose coding is shown in Table 4-8, is used to set the AO XT board into a self test/calibrate mode. The test mode is entered by S1, position 1 in the OFF position. Position 2 OFF is a ramp output, ON is a high/low output determined by switch position 3 (ON is low, OFF is high output). Switch position 3 used in RAMP (position 2 OFF) is off for fast ramp, on for slow ramp.

Table 4-8 AO XT Test Switch (SW1) Positions

Switch Position			Test Function	
1	2	3		
Off	Off	Off	Ramp Test	Fast
Off	Off	On		Slow
Off	On	Off	Hi	
Off	On	On	Lo	
On	N/A	N/A	Normal	

4.8 Digital Outputs

The Baseboard supports two different types of digital outputs; SBOs or general purpose digital outputs. There are 8 relay sockets on the Baseboard. These can be used as 4 Select Before Operate (SBO) points or as 8 Digital Output (DO) points. If SBO XTs are used then all relays on the Baseboard must be assigned as SBOs. Connect SBO XTs and DO XTs to J4 (Bank 1) & J3 (Bank 2).

4.8.1 Select Before Operate

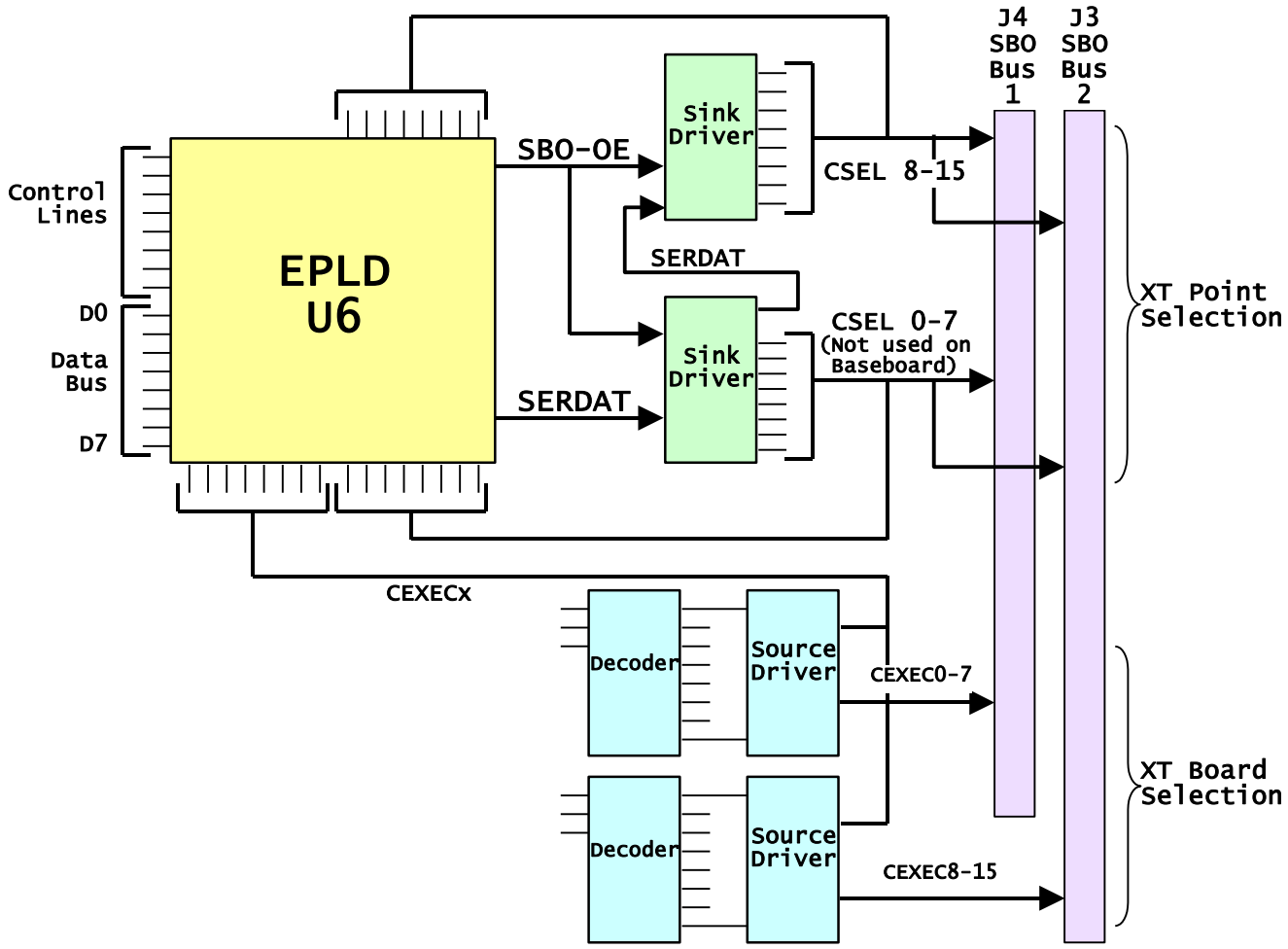
The SBO interface uses 16 source drivers (U10, U15) and 16 sink drivers (U11, U16). The source drivers can only be selected one at a time. A serial-in, parallel-out shift register feeds the 16 sink drivers, and allows all the sink drivers to be asserted simultaneously if desired.

All drivers have feedback resistor networks which allow the RTU to monitor correct relay driver selection before execution is enabled. The SBOs are controlled by an Erasable Programmable Logic Device (EPLD). The sink drivers control the CSEL0 - CSEL15 lines. The source drivers control CEXEC0 - CEXEC15.

The relay driver matrix (16 X 16) can handle a maximum of 256 relays or 128 SBO points. Each SBO consists of a TRIP and a CLOSE relay. It is possible to drive 16 DO relays simultaneously, but SBOs are limited to one at a time by hardware and firmware.

The 8 Baseboard relays use the address of the last half of the first group of 16 relays. Sixteen SBO XT boards (16 relays each) can be added if no SBO relays are used on the Baseboard.

Figure 4-8 SBO Block Diagram



4.8.2 Select Before Operate XT

Refer to the following schematic drawings located in the SAGE 2000 RTU Operation & Maintenance Manual:

- C3133-002-Rev-X, Schematic LD SBO Control 8 T/C Pts
- C3233-002-Rev-X, Schematic M/1C SBO Control 4 T/C Pts
- C3247-002-Rev-X, Schematic M/1C Latching SBO XT 8Pt

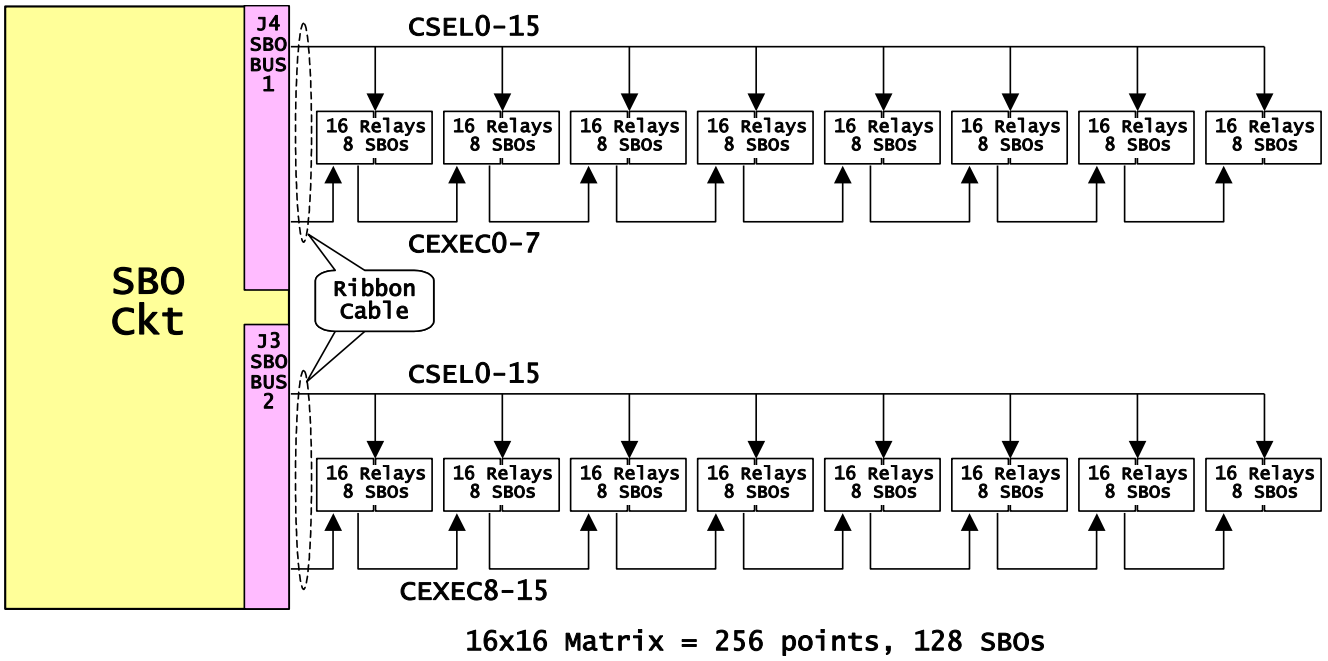
The C3133 SBO XT provides 8 controls (16 relays) on a 8.75 X 19 inch board. Sixteen XTs (128 points) can be connected to the RTU if baseboard SBOs are not used (skipped). Only fifteen SBO XTs can be used if the baseboard SBOs are used (for a total of 124 points).

The reason you must skip the Baseboard SBOs in order to get the full complement of 128 SBOs is because, to make SBO addressing contiguous, SBO addressing for Bank A begins at the second half of a theoretical group of eight SBOs on the baseboard (see Table 4-9). Since we can have only eight groups of eight SBOs, including baseboard SBOs limits the number of XTs to seven for Bank A. So, we would have 7 x 8 + 4 (on the baseboard) = 60 for Bank A. Bank B would yield 64, bringing the total to only 124.

The C3233 panel mount XT can have 8 KUP momentary or 4 KUL latching relays installed. KUEP type relays may be used for high current applications. The C3247 panel mount XT can have 4 or 8 KUL latching relays. This XT provides 2 Form C contacts per point.

Another view of SBO addressing is shown in Figure 4-9.

Figure 4-9 SBO Matrix



The Execute/Select column is based on the schematic. The digit before the "/" is the Execute number. The digit after the "/" is the Select number. For example, 0/8 CEXEC0/CSEL8. This combination is point 1 Trip.

Table 4-9 SBO Relay Assignments with Baseboard Enabled

Location	SBO Database Relay #	Sequential Relay #	Execute/Select	Comments
			0/0 to 0/7	do not exist
	1 trip to 4 close	1 to 8	0/8 to 0/15	baseboard relays
Bank 1 J4	5 trip to 12 close	9 to 24	1/0 to 1/15	1st 16-relay SBO XT
	13 trip to 20 close	25 to 40	2/0 to 2/15	2nd 16-relay SBO XT
	21 trip to 28 close	41 to 56	3/0 to 3/15	3rd 16-relay SBO XT
	29 trip to 36 close	57 to 72	4/0 to 4/15	4th 16-relay SBO XT
	37 trip to 44 close	73 to 88	5/0 to 5/15	5th 16-relay SBO XT
	45 trip to 52 close	89 to 104	6/0 to 6/15	6th 16-relay SBO XT
	53 trip to 60 close	105 to 120	7/0 to 7/15	7th 16-relay SBO XT
Bank 2 J3	61 trip to 68 close	121 to 136	8/0 to 0/15	8th 16-relay SBO XT
	69 trip to 76 close	137 to 152	9/0 to 1/15	9th 16-relay SBO XT
	77 trip to 84 close	153 to 168	10/0 to 2/15	10th 16-relay SBO XT
	85 trip to 92 close	169 to 184	11/0 to 3/15	11th 16-relay SBO XT
	93 trip to 100 close	185 to 200	12/0 to 4/15	12th 16-relay SBO XT
	101 trip to108 close	201 to 216	13/0 to 5/15	13th 16-relay SBO XT
	109 trip to116 close	217 to 232	14/0 to 6/15	14th 16-relay SBO XT
	117 trip to 124 close	233 to 248	15/0 to 7/15	15th 16-relay SBO XT

The Execute/Select column is based on the schematic. The digit before the "/" is the Execute number. The digit after the "/" is the Select number. For example, 0/8 CEXEC0/CSEL8. This combination is point 61 Trip.

Table 4-10 SBO Relay Assignments with Baseboard Disabled

Location	SBO Database Relay #	Sequential Relay #	Execute/Select	Comments
Bank 1 J4	1 trip to 8 close	1 to 16	1/0 to 1/15	1st 16-relay SBO XT
	9 trip to 16 close	17 to 32	2/0 to 2/15	2nd 16-relay SBO XT
	17 trip to 24 close	33 to 48	3/0 to 3/15	3rd 16-relay SBO XT
	25 trip to 32 close	49 to 64	4/0 to 4/15	4th 16-relay SBO XT
	33 trip to 40 close	65 to 80	5/0 to 5/15	5th 16-relay SBO XT
	41 trip to 48 close	81 to 96	6/0 to 6/15	6th 16-relay SBO XT
	49 trip to 56 close	97 to 112	7/0 to 7/15	7th 16-relay SBO XT
	57 trip to 64 close	113 to 128	0/0 to 0/15	8th 16-relay SBO XT
Bank 2 J3	65 trip to 72 close	129 to 144	8/0 to 8/15	9th 16-relay SBO XT
	73 trip to 80 close	145 to 160	9/0 to 9/15	10th 16-relay SBO XT
	81 trip to 88 close	161 to 176	10/0 to 10/15	11th 16-relay SBO XT
	89 trip to 96 close	177 to 192	11/0 to11/15	12th 16-relay SBO XT
	97 trip to 104 close	193 to 208	12/0 to 12/15	13th 16-relay SBO XT
	105 trip to112 close	209 to 224	13/0 to 13/15	14th 16-relay SBO XT
	113 trip to120 close	225 to 240	14/0 to 14/15	15th 16-relay SBO XT
	121 trip to 128 close	241 to 256	15/0 to 15/15	16th 16-relay SBO XT

4.8.2.1 Mixing SBOs & DOs

SBOs and DOs may be mixed on the same RTU by using different buses. Use J3 and J4 for SBO XTs and use the SFB for DO XTs. SBOs and DOs may not be mixed on the SBO bus.

4.8.3 Relay Output

Refer to the following schematic drawings located in the SAGE 2000 RTU Operation & Maintenance Manual:

- C3231-002-Rev-X, Schematic M/1C Digital Output XT 16Pt
- C3243-002-Rev-X, Schematic M/1C Raise/Lower Control BD

When you use the Baseboard relays as parallel outputs (not SBOs), it is necessary to install a shunt on the jumper posts of W15. This shunt bypasses the source driver for CEXEC0, tying the line directly to +24V. This is necessary because the source drivers are incapable of driving 8 relays simultaneously, which may be required for digital outputs. In this case, only the CSELx signals need to be enabled to energize a relay. The CEXC0 signal is used for the baseboard relays or the eighth XT execute if the baseboard relays are disabled.

The DO XT (C3231) is an 8 X 5 board that has 16 digital output relays. This XT is considered to be a half board since two of them can take up the space of a full size, 32 relay XT. Up to eight DO XT boards may be addressed by the SAGE 2400 for a total of 264 output relays including the 8 possible on the Baseboard. The DO, SOE, ACI, SFB AO, and PCI XTs share the special function bus so the aggregate sum of these full sized boards is eight. The relay contacts are capable of switching resistive loads to 10A at 28VDC or 240VAC. A single set of form C contacts are provided for each point. J3 of the first C3231 is cabled to J1 of the second XT. The W1 jumper is placed between pins 1 and 2 of the second half board to be used.

The C3243 is a 19" board with 16 latching relays used for raise/lower controls. A Raise commands latches the Raise relay. Each Raise relay is subsequently unlatched when a Lower command for that channel is executed.

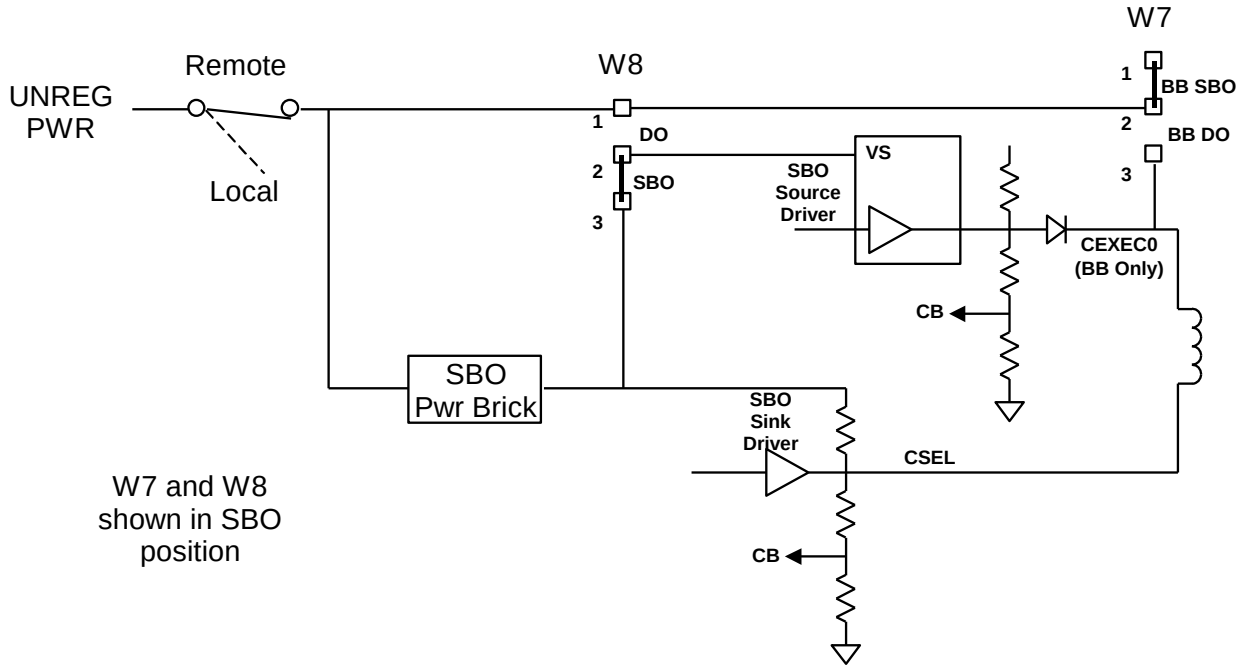
4.9 Summary of SBO/DO Operation

The following options are available when choosing SBO/DO operation:

	W7 DO	W7 SBO
W8 DO	No SBOs anywhere; BB & XT DOs	Do Not Use
W8 SBO	Do Not Use	SBOs

The following simplified circuit diagram shows the relationship between W7 and W8.

Figure 4-10 Jumpers W7 and W8



The Remote/Local switch must be in Remote for either SBO or DO operation. When the jumpers are in SBO position, the small SBO power brick can operate only one relay at a time. In DO position, there is enough power to operate multiple relays at once.

4.10 Digital Input

The digital input subsystem accepts contact closure inputs as field status or low speed accumulator inputs. All inputs are optically isolated, and debounced by the firmware. Input processing is determined by the input assignment as status, accumulator, etc. and is also firmware controlled. This allows the same hardware to be used for both types of inputs. Figure 4-11 is a simplified schematic of a typical digital input.

The Baseboard has 16 digital inputs that can be expanded to 232 with DI XTs. Digital input loops may be powered by 24VDC, 48VDC or 129VDC with appropriate current limiting loop resistors. TB2 and TB5 are the termination blocks for the baseboard digital inputs. These are Phoenix type MSTB, a compression type terminal for 12 to 28 gauge wire.

The baseboard digital inputs are organized in 2 banks of 8 bits. The baseboard digital inputs are interfaced to the data bus DI-D0 to DI-7 by U1 and U2 while the external CH-1 to CH-16 status is buffered by U8. Address lines B-SBSEL1 to B-SBSEL7 (U7 & U40) select the Digital Input XTs. Signals B-LS-A0 and B-

LS-A1(U7) select 1 of 4 eight bit groups of status for each board select (B-SBSELx). Data is allowed to settle before data onto the bus is read. A new status bank is selected by reading the I/O address of the requested status bank, ignoring the data, reading the same I/O address, again ignoring the data, then processing the data.

4.10.1 Firmware Debounce Algorithm

The Digital Inputs are processed through a digital filter to prevent erroneous Changes Of State (COS) being reported because of contact bounce. The inputs are sampled each 5 msec. Any input that does not match the state of the previous scan is time stamped and stored as a possible COS. A 20 msec counter is started for the suspect input. When the 20 msec expires, the point is again sampled. If it has remained steady it is considered to be a valid COS. The COS flag is set and the status buffer is set to the new point condition. A hardware RC network on each digital input provides additional filtering.

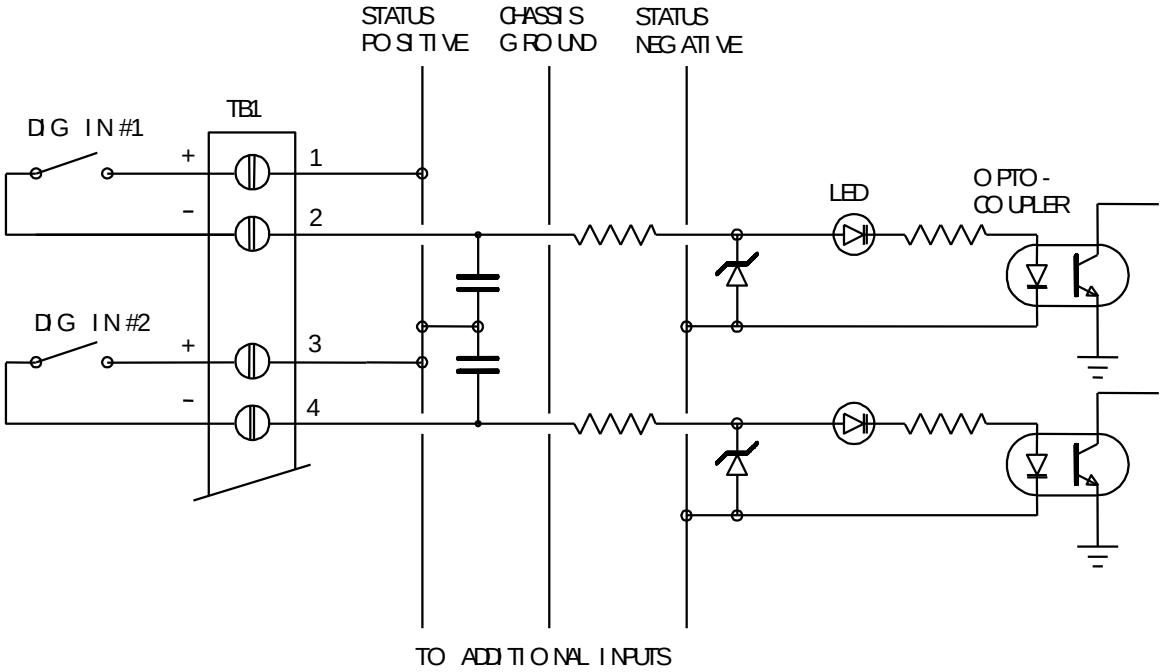
4.10.2 Digital Input XT

Refer to the following schematic drawings located in the SAGE 2000 RTU Operation & Maintenance Manual:

- C3432-002-Rev-X, Schematic M1C 32CH DIN-XT
- C3232-002-Rev-X, Schematic M/1C Digital Input XT 16PT
- C3232-IS2-Rev-X, Schematic M/1C ISOL Digital IN XT 16PT

The Digital Input XTs are supplied as a 32 input 8 X 5 inch board (C3432), and as 16 input 8 X 5 inch boards (C3232 and C3232-IS2). The C3232 IS2 XT allows selection of individual excitation inputs for each circuit. Each DI XT input is optically isolated and provided with an input RC filter. Additional debounce filtering is done in firmware. An address enable is decoded on the XT for each group of eight inputs. The decoder is in turn enabled by the board select (SBSEL0). The board select signals (SBSEL0-7) are rotated on the board so that the next board receives its board select on pin 11 of J1. The C3232 XT has a jumper select to indicate if it is the first or second board of a 16 input pair. This allows two 16 input boards to be used in place of one 32 input XT.

Figure 4-11 Typical Digital Input



4.10.3 1 MSEC SOE

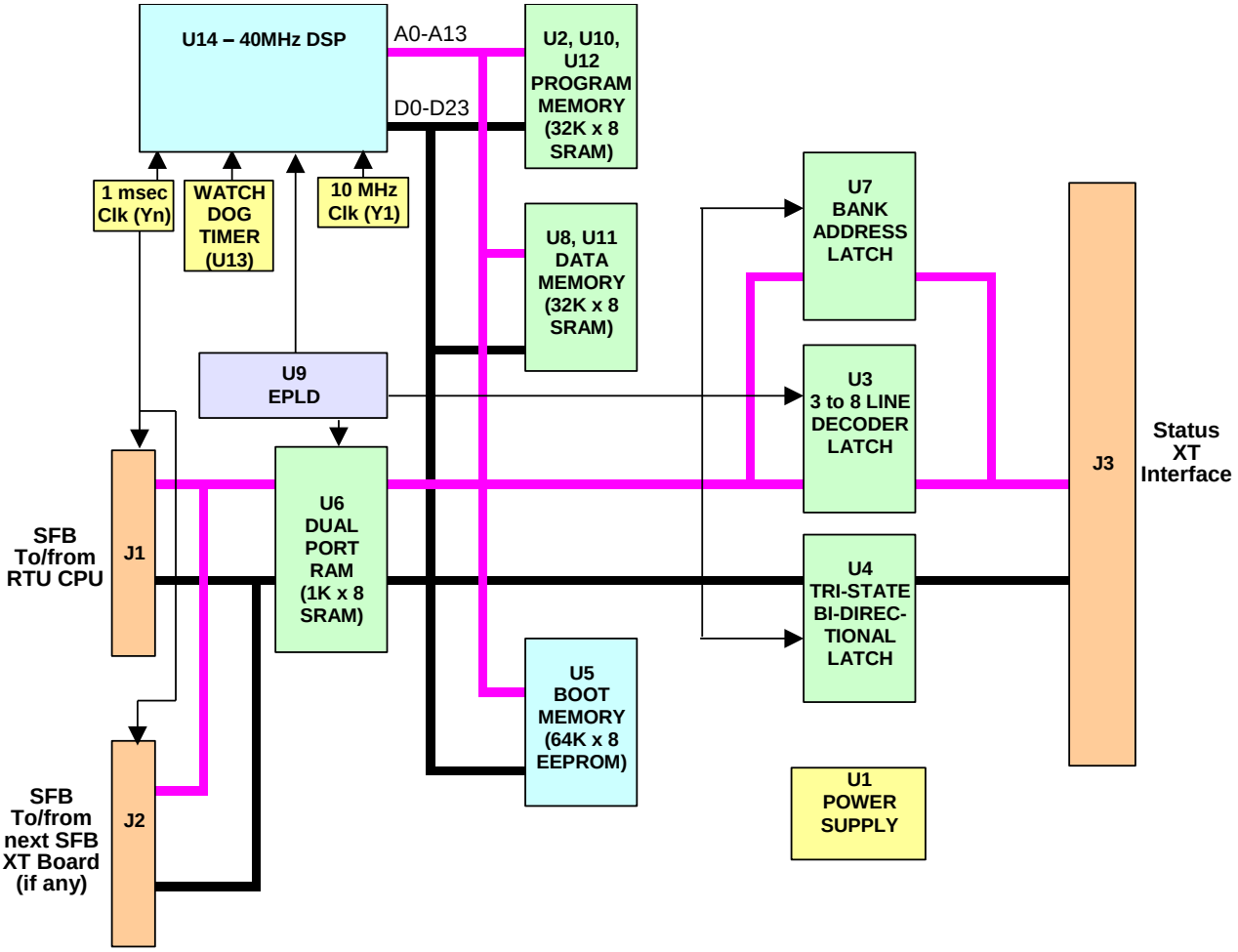
Refer to drawing no. C3235-002-Rev-X, Schematic M/1C 1ms SOE XB, located in the SAGE 2000 RTU Operation & Maintenance Manual, and also to Figure 4-12.

The 1 MSEC-SOE expansion board is an 8" x 5" card that attaches to the Special Function Bus. This card gathers and time tags events with a 1msec resolution. There are no digital input terminations on the C3235 board. C3432, C3232 or C3132 types of DI XTs are directly connected to the SOE board. The input data is conditioned by the SOE and then passed to the Baseboard via the SFB.

The SOE processor is an Analog Devices ADSP-2105. The 2105 is a Digital Signal Processor (DSP). This processor was chosen for its speed and versatility. This is a 10MIPS machine at one instruction every 100nsec. The SOE can gather data on 128 points with a yield of 78 instructions per point per msec. Some of the features of 1 MSEC SOE expansion board are:

- SFB interface
- 8" x 5" format
- meets SWC requirements
- DI via DI XT interface
- 40 MHz DSP (10MIPS)
- 128 points per card
- 3 cards per Baseboard
- +5V power from +24V source
- ±1ppm temperature compensated precision crystal available

Figure 4-12 SOE XB Block Diagram



4.10.4 Pulse Counter Input

The 2 high speed Pulse Counter Inputs (PCI) on the Baseboard are provided by an EPLD in addition to opto-isolators and debounce circuits. Excitation power for the PCI points is provided by the status input point excitation source. Excitation power for PCI XTs should be taken from the baseboard status XT excitation output connector to take advantage of the fuse on the Baseboard. Excitation power for XT board PCI points is input on a pair of terminals for this purpose.

The PCI points are not referenced to ground on the input side of the opto-isolators; they are DC isolated as a group, but not individually. The Baseboard PCI points share group isolation with the status input points, as they use the same excitation source. This configuration is intended for use with dry (non-excited) contacts, and can also be used in other configurations with source voltage.

An LED is provided for each point. DS17 and DS18 illuminate respectively when input 1 and input 2 are active. Debouncing is selectable for each point. A cutoff frequency of approximately 30Hz is appropriate for most relay or other mechanical contacts operating at typical low rates of speed. The cutoff frequency of 1kHz is appropriate for fast mechanical contacts and most semiconductor outputs. A minimum of 10kHz is selected when no filtration jumpers are provided.

4.10.5 Pulse Counter Input XT

Refer to drawing C3250-002-Rev-B, 8-Point High Speed PCI Schematic XT, located in the SAGE 2000 RTU Operation & Maintenance Manual.

The high speed PCI XT is a 8 X 5 board that contains eight PCI circuits. Each input is conditioned identically to the two Baseboard inputs. All inputs are optically isolated and input filtering is selectable. The XT contains three triple 16-bit down-counters (U11-13), one of which is not used. The counters are not provided with a hardware reset line and will come up with a random number in the counter when they are first powered. Firmware provides the counter initial reset. The registers need to be interrogated at least once every 6.5 seconds to avoid losing counts due to an overflow condition at the maximum rate of 10kHz.